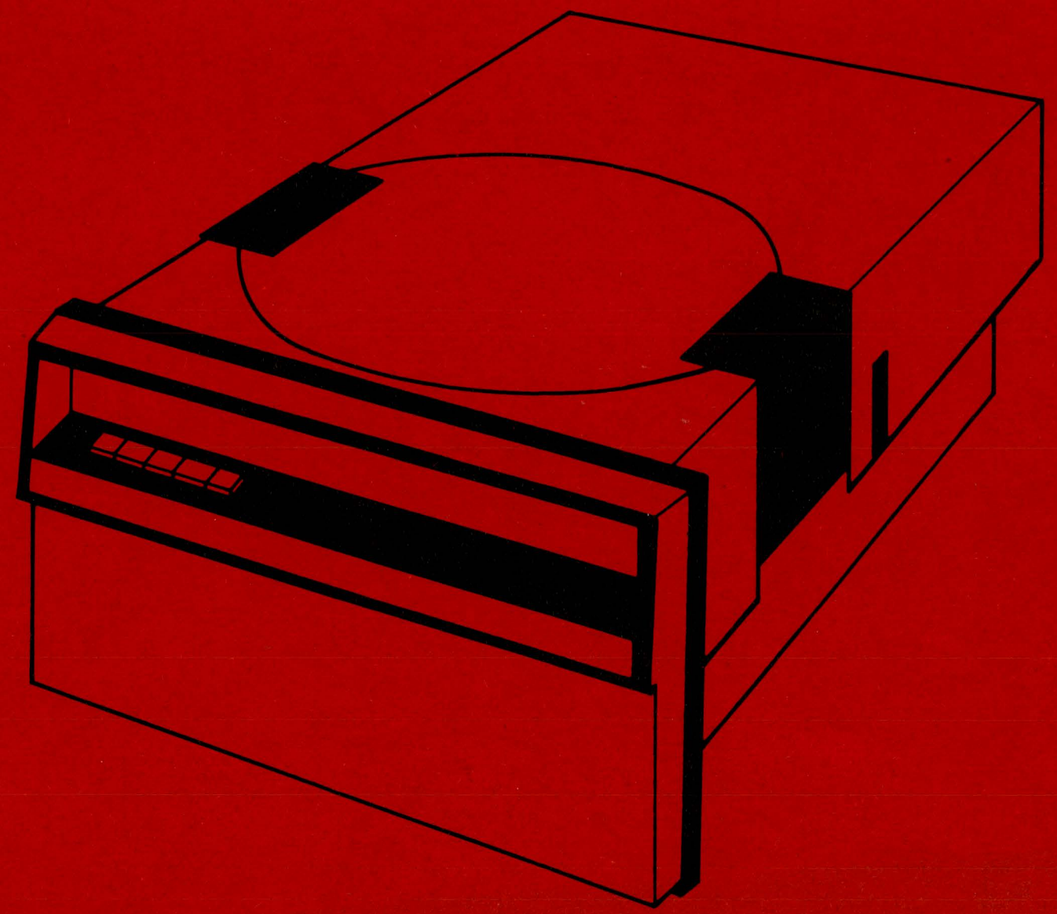
Data Systems

PHILIPS

P800M Service Manual

P824-040 Disc Control Unit



P800M Service Manual

P824-040 Disc Control Unit

The information contained in this manual is based on the documentation available at the time of printing, April 1975. However, should any errors or omissions be discovered, or should any user wish to make any suggestions for improving this manual, he is invited to send his comments to:

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GENERAL DESCRIPTION

1.1

The P852M X1215 CDD Disc Control Unit provides the interface between a P800M CPU and up to two X1215 CDD Disc Drive Units. This section gives general information about the Control Unit (CU), the disc drive unit, and the data organization on the disc; Section II describes the logic of the CU.

1.2 PHYSICAL

The control and interface logics are contained on one CPU size printed circuit card that can be plugged into any CU slot in either the CPU or extention cabinets. Interface between the CU card and the CPU is via connector 3 (of the card) and the GP bus. Control and data signals between the CU and the disc drive units are sent via connector cables: connector 1 (of the card) provides the interface for drive unit 0, and connector 5 (of the card) provides the interface for drive unit 1.

1.3 DISC DRIVE UNIT

The X1215 CDD disc drive unit has one fixed disc and one removable discpack. Table 1-1 gives a brief specification of the drive unit. The drive unit contains the mechanisms, electrical controls and indicators to initiate, perform and indicate completion of the commands sent to it from the CU and is mounted in a standard 19 inch rack mounting cabinet.

Table 1-1 Drive Unit Specification

	Specification
Number of Discs	2 - 1 fixed disc 1 removable discpack
Number of Cylinders per Disc	200 plus 4 spare
Number of Tracks per Cylinder	4 (2 per disc)
Number of Sectors per Track	16
Number of Heads	4 (2 per disc)
Head Positioning Time	60ms Max. (204 cylinders moved) 10ms Min. (1cylinder moved) 30ms average
Latency	12.5ms (half revolution time)
Recording Technique	Double Frequency
Recording Density	2200bpi
Serial data transfer rate	2.5M bits per second nominal at 2400rpm

1.4 DISC ORGANISATION

The recording area of each disc is organised into cylinders, tracks and sectors. Data is written or read serially in groups of 16 bit words called a record, and there is one record per sector.

1.5 Cylinders

There are 204 concentric tracks per disc surface and a track position common to the four disc surfaces is called a cylinder. The cylinders are numbered from 0 to 203 starting at the outer edge of the disc and moving towards the center. Only 200 of the cylinders are addressable by program, the other four cylinders provide four spare tracks for each disc surface in case defects occur on any of the other tracks.

1.6 Tracks

There are 200 programmable tracks on each disc surface and the length of each track is one revolution of the disc. The drive unit sends an index pulse to the CU for each revolution of the disc. These index pulses are used by the CU to synchronize the sector pulses.

1.7 Sectors

Each revolution of the disc is divided into sixteen sectors by 16 evenly spaced sector pulses that are sent from the drive unit to the CU to synchronize read/write operations. The sectors on the upper surface of each disc are numbered 0 to 15, and the sectors of the lower surface are numbered 16 to 31. Each sector has a physical identifier (provided by the sector pulses), and a software identifier supplied by program. These software identifiers are interlaced with the physical identifiers to ensure a fast transfer rate. Figure 1-1 shows the relationship between the index pulse, the sector pulses and the physical and software identifiers.

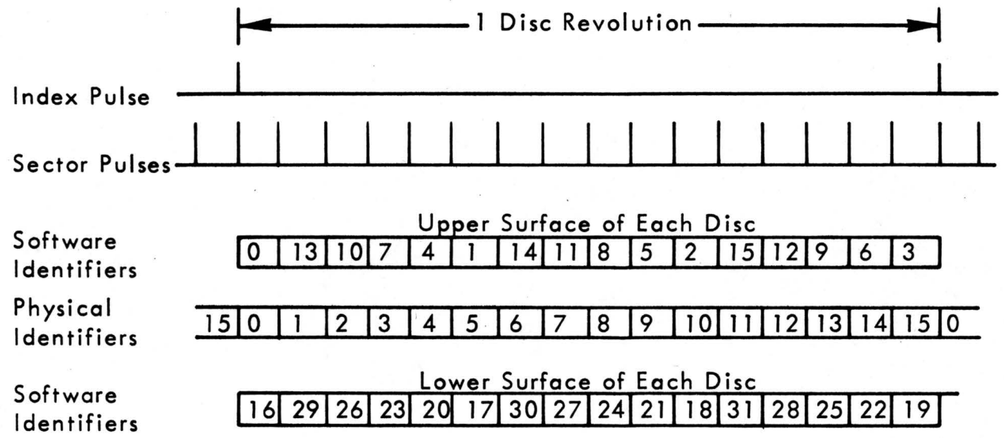


Figure 1-1 Index and Sector Pulses with Physical and Software Identifiers

1.8 Records

A record is a variable length data block of 16 bit words and is contained in a single sector. The maximum number of data words per record is 208 and the first word of each record must be the identifier.

1.9 Record Format. The data words of a record are written/read serially, the most significant bit of each word being written/read first. The format of each record is:

where --

- Gap is a length of 51.2 μ sec (8 words long) used to prevent overlapping between sectors and to allow time for the required head to be selected.
- Synchronization Area is 18 words long and each word contains 16 data zero bits. It is written at the beginning of each rite command by the CU. During ead commands it is used to obtain bit synchronization before reading the preamble, and reading begins in the theoretical middle of the synchronization area.
- Preamble is one word with the following bit pattern, 0000000000000001 and is used to synchronize the read command.
- Data Words is a number of words determined by program up to a maximum of 208 including the identifier.
- LRC is the Longitudinal Redundancy Check word. The LRC is hardware generated during Write commands and is an Exclusive-OR of all the data words in the record plus the identifier. During Read commands an Exclusive-OR of the record is again made by hardware and compared with the LRC. If they are different, a data fault has occurred and the appropriate status bit is set. The LRC is never sent to the CPU.
- Postamble is 16 zero bits and is used to indicate the end of a record.
- Erase Delay is 6 words long (the distance between the read/write and erase heads) and enables the erase head to tunnel erase the track to the end of the record.

1.10 Recording Technique

The drive unit uses the double frequency recording technique to write data on the disc. The CU sends clock pulses to the selected head, on the selected drive unit, at a frequency of 2.5 M bits per second and there is one clock pulse for each data bit. For each data one bit a 100 ns data pulse is recorded as the clock pulse; data zero bits are not recorded. Figure 1-2 shows an example of the clock and data pulses.

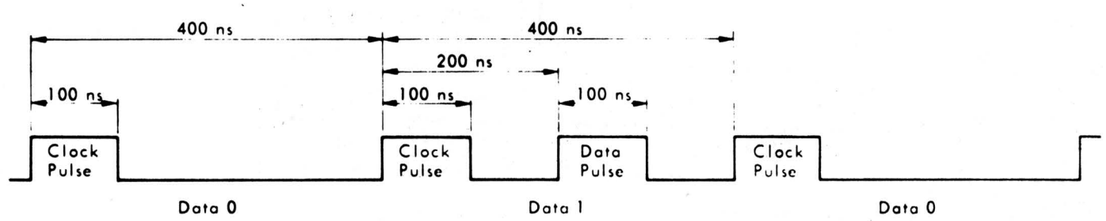


Figure 1-2 Example of Recording Technique

1.11 DRIVE UNIT AND HEAD SELECTION

The information to select the required drive unit, head and disc is contained in each of the I/O instructions. When the CU receives and accepts an I/O instruction it activates the selection logic and sends the appropriate commands to the selected drive unit.

1.12 Drive Unit and Disc Selection

This information is received on MAD10 and MAD11. MAD10 indicates the selected disc and MAD11 indicates the selected drive unit as shown below:

MAD10	MAD11	Drive Unit	Disc
0	0	0	Discpack
1	0	0	Fixed
0	1	1	Discpack
1	1	1	Fixed

1.13 Head Selection

There are four heads, one per surface for each disc. All four heads are controlled and positioned by one actuator so the four heads are always on the same cylinder. The CU takes the information on BIO09 and MAD10 and uses it to select the required head as shown below:

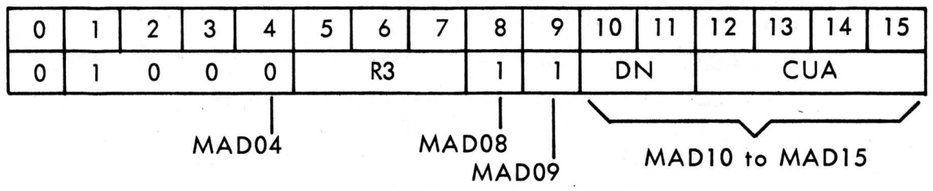
BIO09	MAD10	Head	Disc	Surface
0	0	0	Discpack	Upper
1	0	1	Discpack	Lower
0	1	2	Fixed	Upper
1	1	3	Fixed	Lower
BUS00	BUS01	BUS lines strobed by Head SELECT		

1.14 I/O INSTRUCTIONS

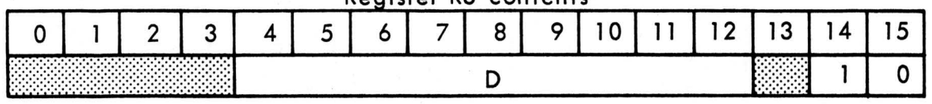
The CU recognizes and is activated by the seven I/O instructions described in the following paragraphs. When these instructions are recognized and accepted, the CPU condition register is reset to 0. If the instruction is not accepted, the condition register is set to 1. Any instruction with a non-recognizable device address sets the condition register to 3.

1.15 Seek Command

This command is used to move the heads from one cylinder to another and it is possible to perform a seek with a displacement which is nul if the heads are already on the required cylinder. The format of the instruction is:



Register R3 contents



BIO Lines

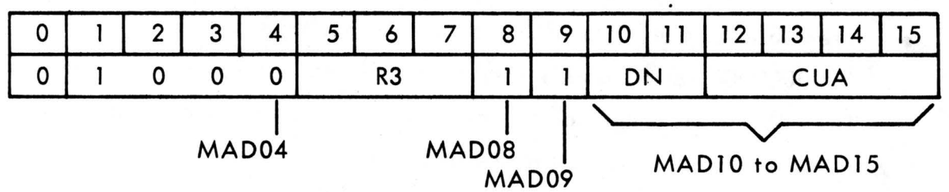
where --

- DN is the drive unit number and is indicated by MAD11.
- CUA is the control unit address and is indicated by MAD12 to MAD15.
- D indicates the cylinder number.
- BIO14 and BIO15 indicate the Seek command.

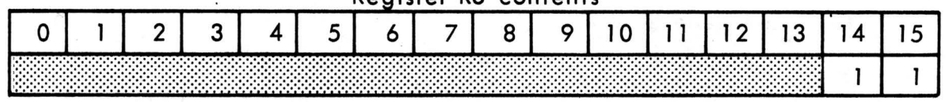
The first word of each record is a software identifier that contains the cylinder number. When either reading or writing a record it is possible to check that the heads are on the correct cylinder by reading the identifier of the preceeding record. A special program writes these identifiers on each sector the first time a disc is ever used. It starts at sector 0 of cylinder 0 and ends at sector 31 of cylinder 203. The program also check reads the disc to make sure that all sectors and cylinders have an identifier as the first word in each data field.

1.16 Seek to Zero Command

This command is the same as a normal Seek command except that the heads are moved from any cylinder to cylinder zero. The format of the instruction is:



Register R3 contents



BIO Lines

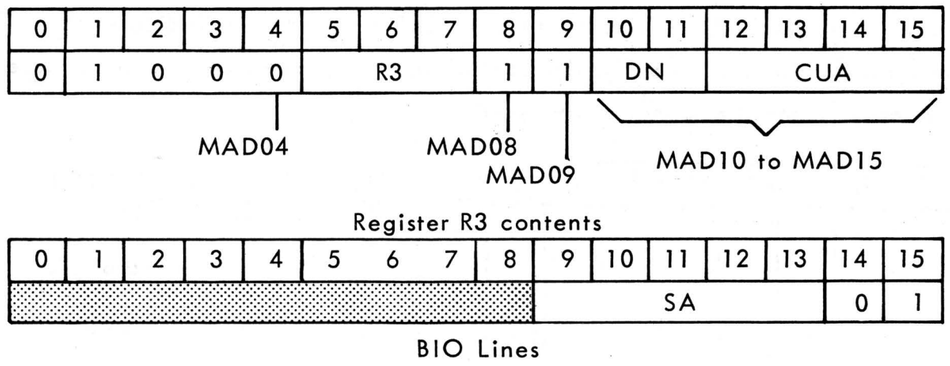
where --

- DN is the drive unit number and is indicated by MAD11.
- CUA is the control unit address and is indicated by MAD12 to MAD15.
- BIO14 and BIO15 indicate the Seek to Zero command.

1.17 Write a Sector Command

This command is used to start a Write command, on the sector addressed by the BIO lines, on the cylinder selected by the previous Seek command.

The format of the instruction is:

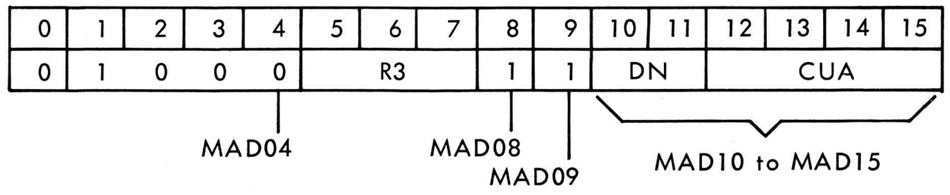


where --

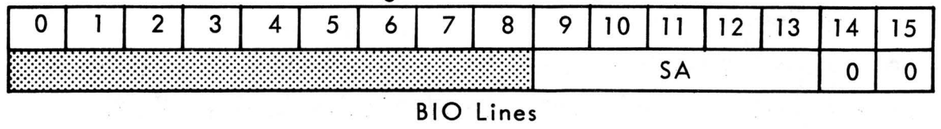
- DN is the drive unit and disc selection. MAD10 indicates the selected disc, and MAD11 indicates the selected drive unit number.
- CUA is the control unit address and is indicated by MAD12 to MAD15.
- SA is the sector and head selection. BIO09 indicates the selected head and together with BIO10 to BIO13 indicates a sector address from 0 to 31.
- BIO14 and BIO15 indicate the Write command.

1.18 Read a Sector Command

This command is used to start a Read command, on the sector addressed by the BIO lines, on the cylinder selected by the previous Seek command. The format of the instruction is:



Register R3 contents



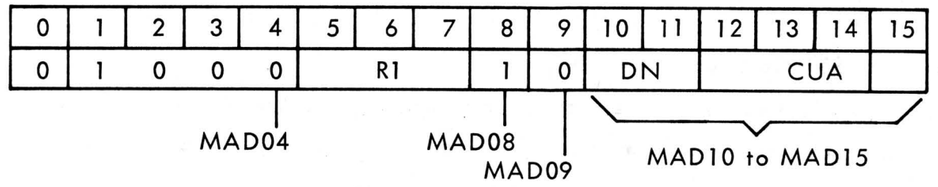
where --

- DN is the drive unit and disc selection. MAD10 indicates the selected disc, and MAD11 indicates the selected drive unit number.
- CUA is the control unit address and is indicated by MAD12 to MAD15.
- SA is the sector and head selection. BIO09 indicates the selected head and together with BIO10 to BIO13 indicates a sector address from 0 to 31.
- BIO14 and BIO15 indicate the Read command.

1.19 Stop Command

This command is used to stop any data transfer between the CU and the CPU. If the command occurs during a read or write operation the transfer is stopped and the interrupt that normally follows at the end of a transfer occurs immediately.

The format of the instruction is:



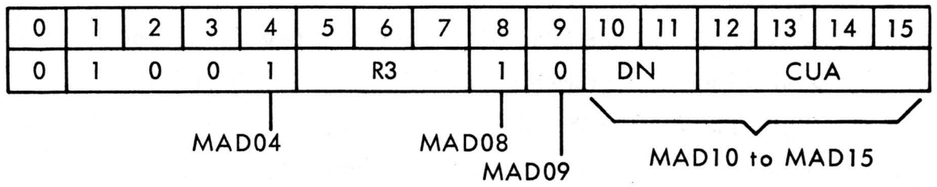
where --

- MAD04, MAD08, and MAD09 indicate the Stop command.
- R1 is not significant.
- DN indicates the drive unit number, but is not significant.
- CUA is the control unit address and is indicated by MAD12 to MAD15.

This command is always accepted by the CU, but it will not affect any seek operation that is in progress.

1.20 TST Command

This command is used to test the status of the control unit before initiating a data exchange. The command is always accepted by the control unit and does not affect any running operation. If the control unit is not busy it responds by filling the status word with all zeros. If the control unit is busy it responds by putting a 1 in bit 15 of the status word. The format of the instruction is:

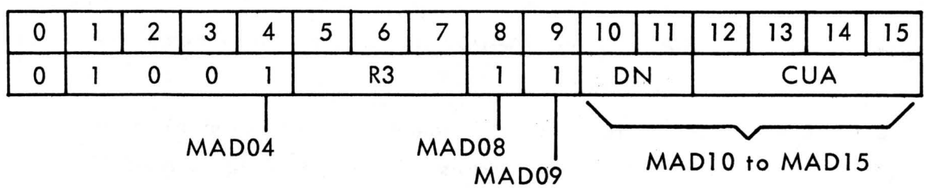


where --

- MAD04, MAD08 and MAD09 indicate the TST command.
- R3 indicates the register into which the status word is to be loaded.
- DN indicates the drive unit number, but is not significant.
- CUA is the control unit address and is indicated by MAD12 to MAD15.

1.21 SST Command

This command is used to get the status word from the control unit at the end of an I/O operation. The command is only accepted in the Wait Status state of the control unit, and the format of the instruction is:

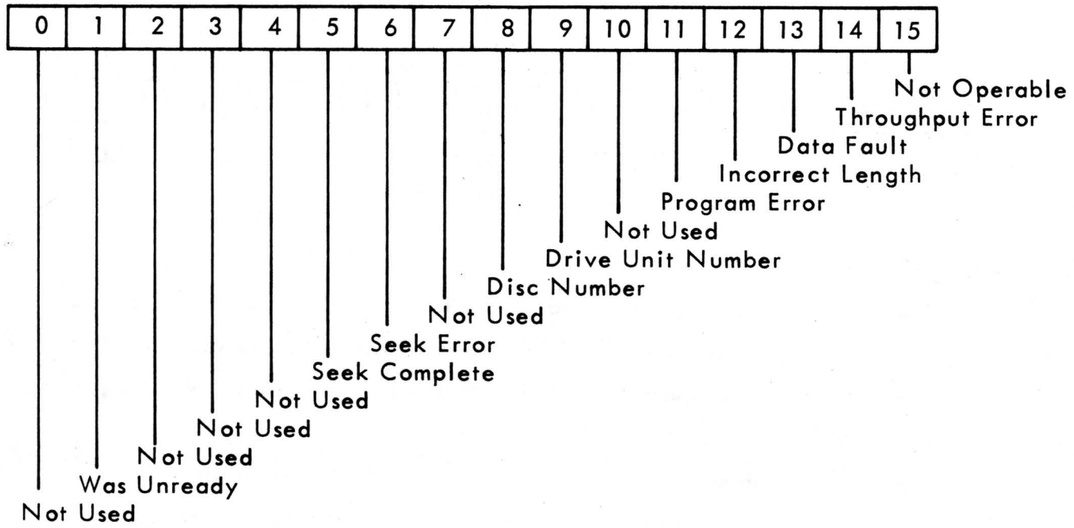


where --

- MAD04, MAD08 and MAD09 indicate the SST command.
- R3 indicates the register into which the status word is to be loaded.
- DN indicates the drive unit number, but is not significant.
- CUA is the control unit address and is indicated by MAD12 to MAD15.

1.22 STATUS WORD

This word is sent to the CPU in response to an SST command. It indicates the various error, and other states, of the control unit and drive units. One or more bits may be set, and the format of the word is:



Each bit of the status word is loaded by the output of a flip-flop; the conditions for setting the bits is given in the following paragraphs.

1.23 Not Operable

Bit 15 is set if the control unit is busy, or if the drive unit is not operable.

1.24 Throughput Error

Bit 14 is set when serialization or deserialization of a data word has ended before the CPU has answered the exchange data request. When this error occurs data exchange requests are inhibited and the control unit switches into the Wait Status state.

1.25 Data Fault

Bit 13 is set when the LRC check fails at the end of either a Read command.

1.26 Incorrect Length

Bit 12 is set during a Read command whenever the physical record length is different from the programmed record length.

1.27 Program Error

Bit 11 is set when an invalid Read or Write command is received. This error stops any further data exchange.

1.28 Drive Unit Number

When drive unit 0 is selected bit 9 is also 0; when drive unit 1 is selected bit 9 is set to 1.

1.29 Disc Number

Bit 8 is 0 if the discpack is selected, and it is set to 1 if the fixed disc is selected (after a read/write operation - after a seek or ready interrupt it will always be 0).

1.30 Seek Error

Bit 6 is set if the seek operation has finished but the heads are not on the correct cylinder, or if the drive unit becomes inoperable during a seek operation.

1.31 Seek Complete

Bit 5 is set when a seek operation has finished, whether it was carried out correctly or not.

1.32 Was Unready

Bit 1 is set during a scanning operation when a drive unit state has changed from inoperable to operable.

1.33 SCANNING

When the CU is in the Inactive state the state of each drive unit is scanned every 6.4 μs. If a change of state is found for either drive unit (e.g. end of seek operation) the scanning is stopped and the CU switches into the Wait Status state with bit 1 of the status word and the drive unit number set. Then the CU sends an interrupt to the CPU.

1.34 LOADING/UNLOADING THE DISCPACK

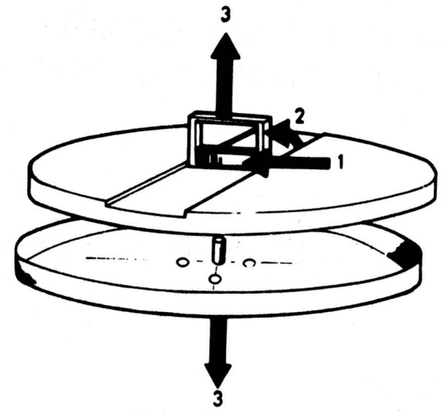
Before loading or unloading a discpack make sure that only the CART. EXCH. and the POWER indicator lamps are lit. Take care not to damage the discpack when carrying out the following operations.

1.35 Loading the Discpack

To load a discpack refer to Figure 1-3 and use the following routine:

- Pull the drive unit out of the rack to the first stop position and open the two clamps by pushing sideways.
- Push the decoupler, in the handle of the discpack, to the left and lift the handle. Then remove the bottom cover and release the decoupler.
- Insert the discpack into the drive unit and fold the handle into its recess (the discpack is correctly loaded when it cannot be rotated or tilted).
- Place the bottom cover, inverted, on top of the discpack and close the two clamps. Then push the drive unit back into the rack.
- o Push the START/STOP button; the drive unit is ready to operate when the READY indicator lights.

1. Push Decoupler to the Left
2. Raise Handle
3. Remove Cover



1. Fold the Handle into its Recess
2. Place the Bottom Cover, inverted, on Top of the Cartridge
3. Close the two Clamps

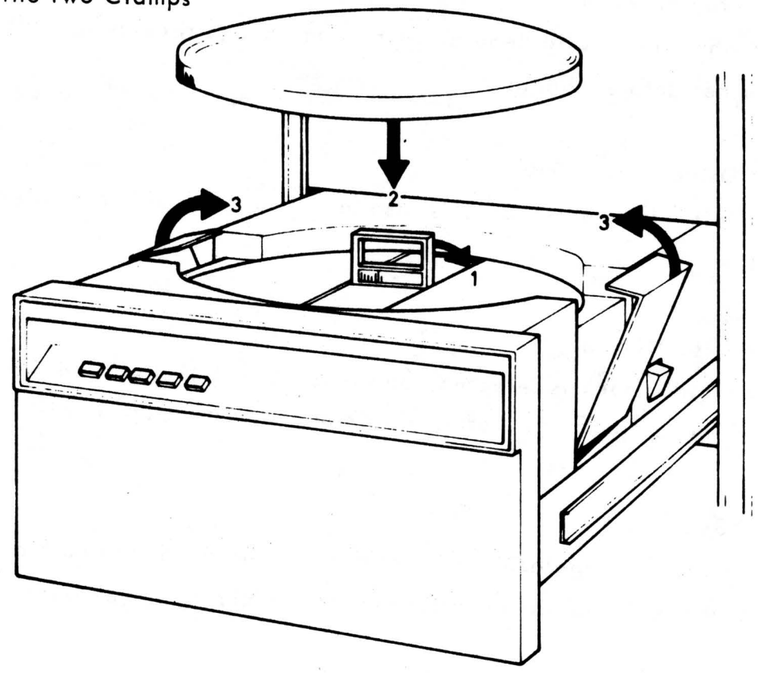


Figure 1-3 Loading the Discpack

1.36 Unloading the Discpack

To unload the discpack refer to Figure 1-4 and use the following routine:

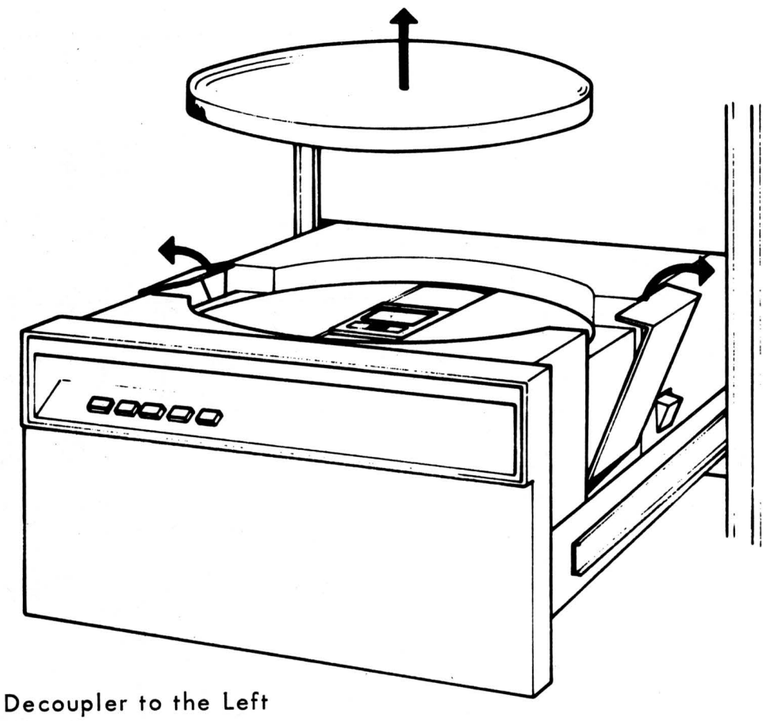
- Stop the drive unit by pushing the START/STOP button and wait until the CART. EXCH. indicator is lit.
- Pull the drive unit out of the rack to the first stop position and open up the two clamps by pushing sideways.
- Remove the bottom cover of the discpack from the drive unit.
- Push the decoupler, in the handle of the discpack, to the left and lift the handle of the discpack to remove the discpack from the drive unit.
- Insert the discpack into its bottom cover and release the decoupler, then push handle into its recess.
- Close the two clamps and push the drive unit back into the rack.

1.37 INTERRUPT PRIORITY ENCODING (BIEC Lines)

Figure 1-5 shows the interrupt priority encoder. The priority levels are numbered from 0 (highest priority) to 63 (lowest priority) in binary, and the required interrupt priority is selected by using the plastic covered U links to select the required binary 0 and 1 levels.

1.38 ADDRESS ENCODING

Figure 1.5 shows the address encoder. The address is encoded in binary by selecting the required 0 and 1 levels with the plastic covered U links. In the figure the U links have been placed to encode address 0010 in binary; the equivalent decimal address is 2. The required address for each CU is selected at system installation time, but may be changed as required by encoding the new binary address using the U links.



1. Push Decoupler to the Left
2. Raise Handle
3. Remove Cartridge by using Handle

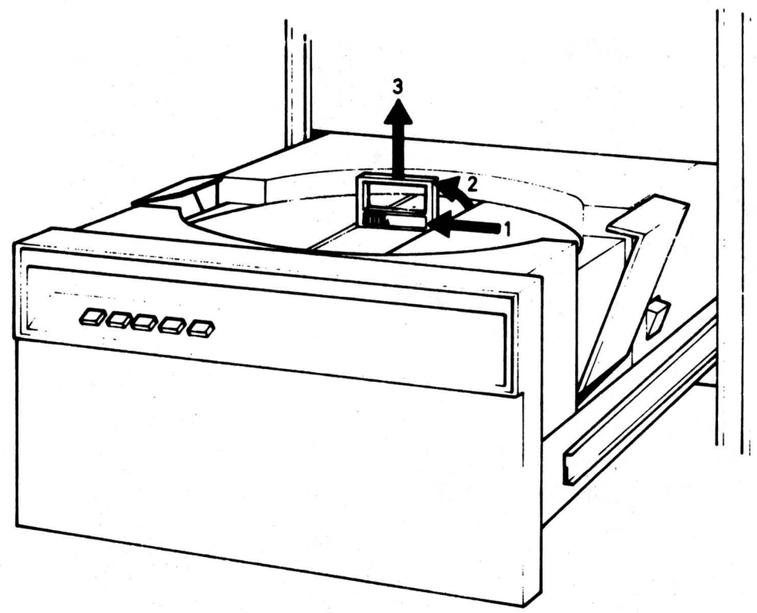


Figure 1-4 Unloading the Discpack

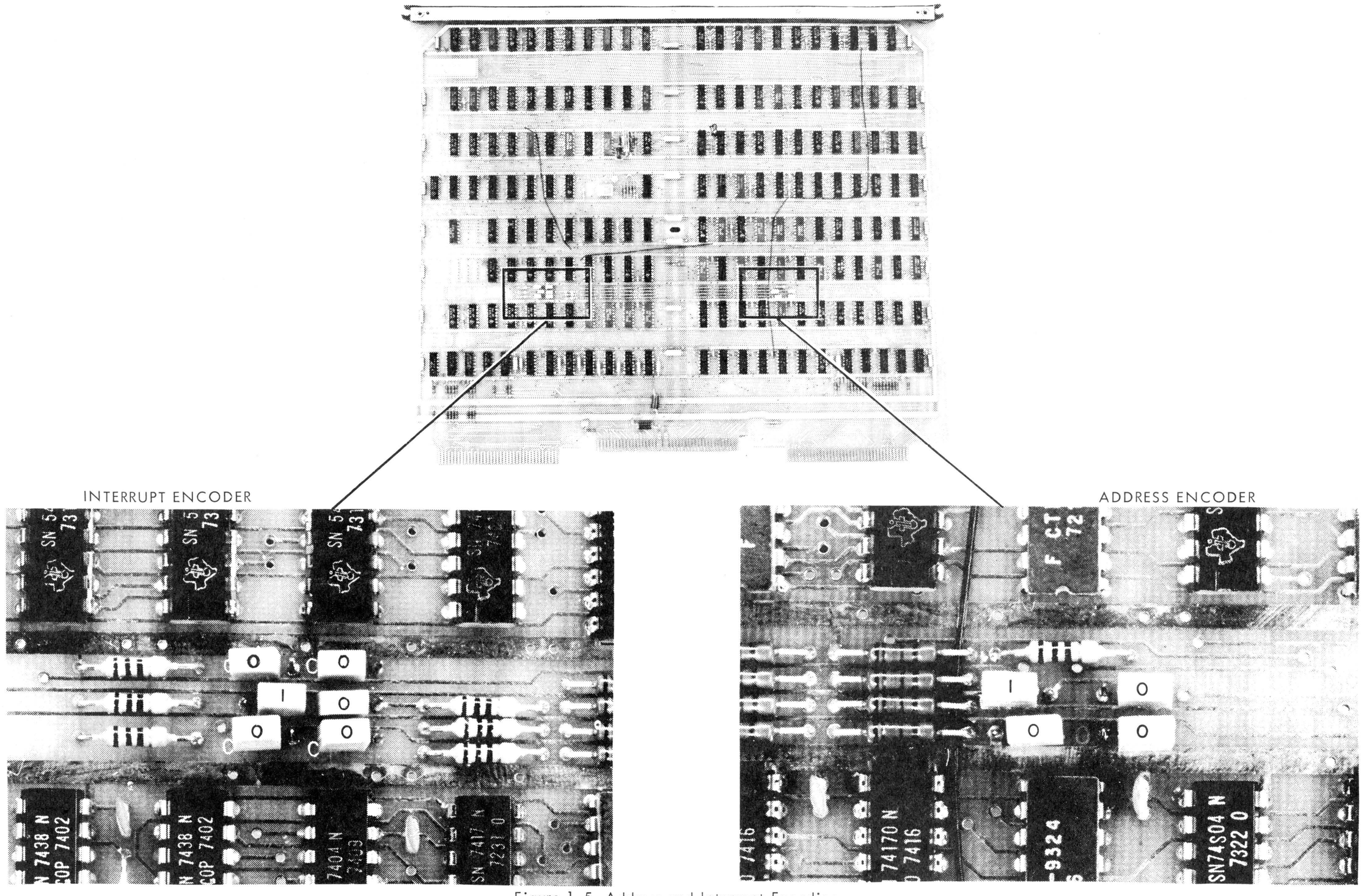


Figure 1.5 Address and Interrupt Encoding

SECTION II

LOGIC DESCRIPTION

2.1

The interface connection between the CU and the CPU is made via connector 3 of the CU printed circuit card, and all I/O transfers and commands are under the control of the I/O Processor Channel (IOP). Interface between the CU and the drive units is made via connectors 1 (drive unit 0) and 5 (drive unit 1) of the CU card and two 50 way cables, one per drive unit. Figure 2-1 shows a block diagram of the main logic blocks and their interconnections. In this diagram the interface signal names, between the CU and the drive units, have been given without reference to either drive unit.

To simplify the logic description, only the main logic element location reference will be given together with the diagram on which it appears e.g. function decode element F3 (Figure 2-7).

2.2 ADDRESS DECODE LOGIC

Element H2 (Figure 2-7) is a five bit comparator that checks the four bit address on MAD lines 12 to 15 against the hardwired address of the CU. When the two addresses are equal, the output from the comparator together with TMPN set the address recognized flip-flop D5 whose output (pin 9) is used to clock the function register and to send the TPMN signal to the CPU. D5 is reset by A2.

2.3 FUNCTION DECODE LOGIC

The I/O commands on the three MAD lines 04, 08 and 09 are decoded by element F3 (Figure 2-7) and stored in the function register elements E5 and F5. All seven I/O commands described in Section I are sent by program from the CPU to the CU, but during data transfers the IOP sends the INR or OTR command to

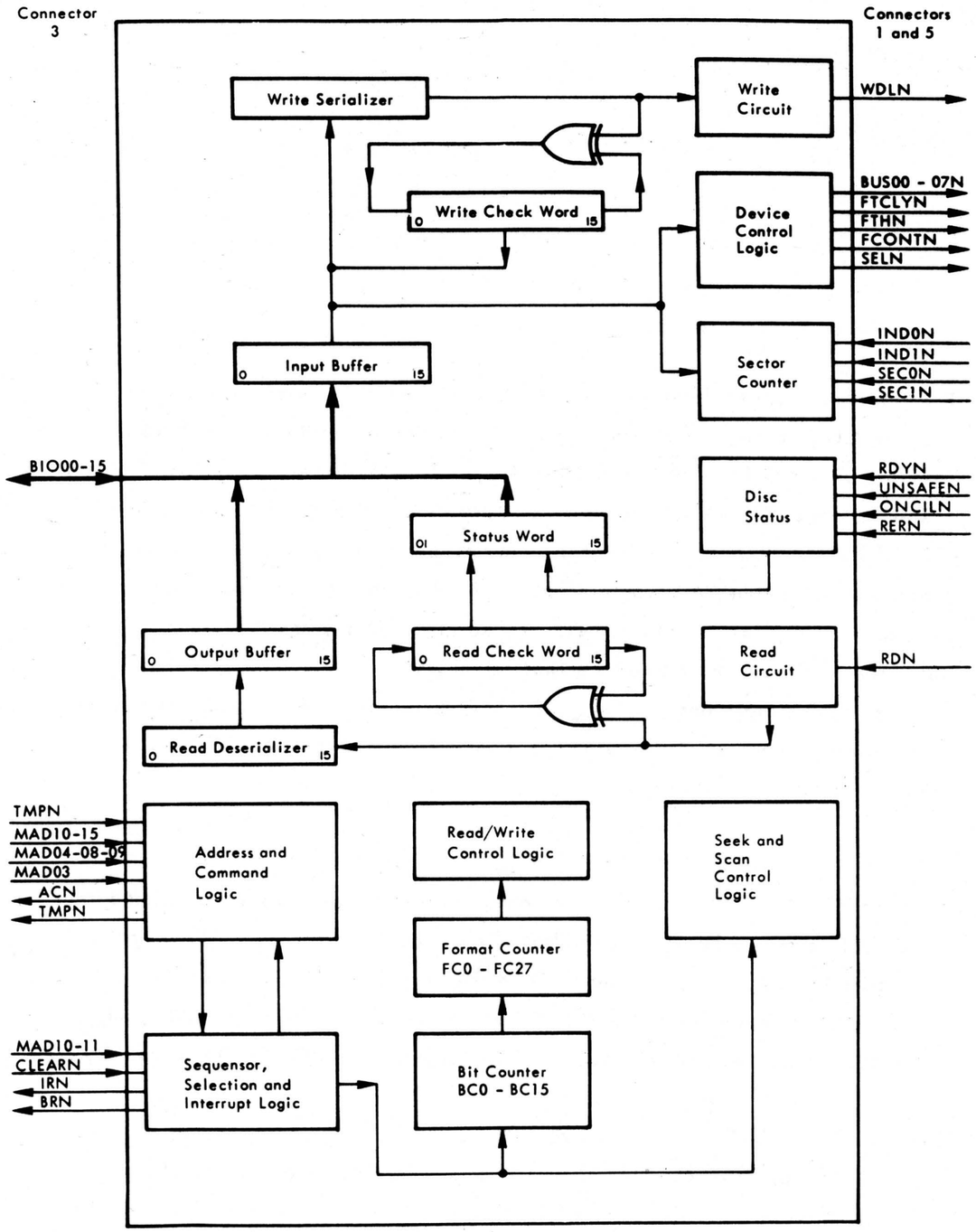


Figure 2-1 Block Diagram of Control Unit

the CU. If the CU interface sequensor is in the correct state and the drive unit is not busy, the CU sends the accept signal ACN to the CPU. The two Seek and the Read and Write commands, from the CPU, also send function information on the BIO lines to activate the drive unit command logic.

2.4 INTERFACE SEQUENSOR

The interface sequensor uses two flip-flops F7 (Figure 2-7) to produce F0 and F1. These signals are used to witch the CU into one of the following four states:

- INCT. Both F0 and F1 are reset by either CLEARN, the trailing edge of an SST command, or when a Seek command has been initiated. In this state the CU is waiting for either a new I/O command or the end of a seek operation.
- EXT. F0 has been reset by the trailing edge of an SST command and F1 has been set by an I/O command. In this state the CU initiates and controls a command to one of the drive units.
- ECH. Both F0 and F1 are set. F0 is set by the Read/Write command and F1 is set by the I/O command. In this state data is gated either to or from the CPU.
- WST. F0 is set and F1 is reset by FHALT. In this state an interrupt is sent to the CPU which responds with an SST command.

2.5 CONTROL FLIP-FLOPS

In addition to the sequensor there are seven other flip-flops that control the operation of the various functions. The operation of these flip-flops is described in the following paragraphs.

2.6 FBR

The break request flip-flop is A2 (Figure 2-12) and it is set for each data word during Read/Write commands. Reset is by ACINR (for Read commands), by ACOTR (for Write commands), by SCAN, or if there has been a throughput error reset is by FBRW=0.

2.7 FCOMP

This is the sector comparator flip-flop S5 (Figure 2-11) and it is set during Read/Write commands by the leading edge of the sector pulse following the addressed sector. It enables the head selection, the Read/Write command, and the serialization/deserialization of a record. It is reset by F1A at the end of a data exchange.

2.8 FEN

This is the enable flip-flop for data serialization V8 (Figure 2-12) and it is set at FC27 time of a Write command and at BC1.FPRE time of a Read command. Reset is by SCANN.

2.9 SCAN

The Scan flip-flop is G8 (Figure 2-7) and it is et each time the CU switches into the INCT state. One output from the flip-flop is used, together with WCP and BC15, to toggle the DA0 flip-flop C5 (Figure 2-12) every 6.4 μs and the output from this flip-flop scans the two drive units. During scanning the following conditions may occur:

- At BC2 time the FST01 flip-flop will be set if a drive unit that was inoperable becomes operable. The FST05 flip-flop is set if ON Cylinder signal is received for a drive unit that was performing a Seek command, and the FST05 and FST06 flip-flops will be set if the seek error (RER) or not operable signals are received for a drive unit performing a Seek command.
- At BC3 time FHALT is set if either FST01 or FST05 are set for a drive unit. The CU then switches into the WST state.

The flip-flop is reset by the leading edge of an accepted CIO instruction.

2.10 FHALT

The halt flip-flop is S5 (Figure 2-12) and it is set if a CIO is attempted on an inoperable drive unit, by a CIO HALT command, by the EOR signal at the end of a Read/Write command, or for any error condition that occurs during any operation. With this flip-flop set, the CU switches into the WST state and sends an interrupt to the CPU. Reset is by ACSST or CLEAR.

2.11 FPRE

The preamble detection flip-flop V8 (Figure 2-14) is set by the first ONE bit that appears on the read data line (the ONE bit of the preamble). It is used to reset the Read Check Word (RCW) register and to enable the Bit Counter BC. Reset is by SCAN.

2.12 FRENA

This is the read enable flip-flop U8 (Figure 2-12) and it is set at FC19 time of a Read command in the theoretical middle of the synchronization area. The output from this flip-flop enables the read circuit to sample the data line from the drive unit. It is reset at the end of a record by SCAN or by FST12 if a sector pulse occurs before the end of the record.

2.13 DRIVE UNIT COMMAND LOGIC

The information to activate the drive unit command logic is sent from the CPU on MAD lines 10 and 11 and on BIO lines 04 to 15 (the contents of the R3 register). Commands to the drive unit are sent via nine BUS lines and three select tag lines once the required drive unit selection logic has been activated.

2.14 Drive Unit Selection

The selected drive unit is indicated on MAD line 11 and is stored in flip-flop D5 (Figure 2-12); logic 0 indicates drive unit 0 and logic 1 indicates drive unit 1. The output from this flip-flop drives flip-flop C5 that produces DA0 and DA0N, and these signals are used to enable the commands to the selected drive unit.

2.15 Disc Selection

The disc selection is indicated by MAD line 10 and is stored in flip-flop F2 (Figure 2-7); logic 0 indicates the discpack and logic 1 indicates the fixed disc.

2.16 BUS Lines

The BUS input is from the BIO line buffer whose output lines are wired to reverse the order of the bit positions. The logic for the BUS lines is shown on Figure 2-9 and the binary bit pattern of the lines is strobed by the select tag lines to activate the control logic in the selected drive unit. Table 2-1 shows the configuration of the BIO lines, the buffer output lines, the BUS lines, and the signals sent to the drive unit.

BIO* Lines	Buffer* Output	BUS Lines	Cylinder Select	Head Select	Control Select
12	3	0	1	0/1	Write Enable
11	4	1	2	2/3	Read Enable
10	5	2	4		Seek
09	6	3	8		
08	7	4	16		Erase Enable
07	8	5	32		Seek
06	9	6	64		Seek to Zero
05	10	7	128		
04	11	8	256 (reserved)		

* Data from these columsn are only valid for a cylinder address: head selection is described in paragraph 1.3.

2.17 Seek Command

The Seek and Seek to Zero commands are indicated by BIO lines 14 and 15 and these signals are used as input to flip-flop F2 (Figure 2-7); BIO lines 14 and 15 indicate the Read/Write commands. Outputs F2 are used to produce FSEEK, FBSEEK and FBSEEKN, and as input to C3 that decodes one of four states. The outputs from C3 are inverted and are: SEEK0, SEEK, READ and WRITE. All these signals are used by the associated control logic in the CU.

2.18 Cylinder Selection

The cylinder address is sent to the drive unit via BUS00 to BUS08 and is gated by FBSEEK. Validation of the address is by the strobe pulse FTCYL which is one output from four-bit latch Y4 (Figure 2-10). On receipt of this pulse the address of the cylinder is memorized by the selected drive unit.

2.19 Seek Operation

Once the cylinder address has been sent to the drive unit, the CU gates the Seek command onto BUS02 and BUS05 (for a Seek to Zero command only BUS06 is sent) with FBS Y4 (Figure 2-10), and the command is validated by the strobe pulse FCONT. This pulse is the output from a flip-flop that comprises Nand gates X5 and X6 (Figure 2-10). The Seek command is completed when the ONCIL signal R8 (Figure 2-10) comes back from the selected drive unit. Figure 2-2 shows an example of a seek operation.

2.20 Write Command

When the required sector is found on the addressed drive unit and disc, the CU gates the selected head number onto BUS00 and BUS01 with FBSEEKN which is enabled by FBUSLN Y4 (Figure 2-10) from BC1 to BC8. The head number is validated by the FTH strobe pulse Y4 from BC3 to BC6 time. At FC8 time the Write and Erase signals are gated onto BUS00 and BUS04 by FBWGN and FBRW respectively.

2.21 Read Command

When the required sector is found on the addressed drive unit and disc, the CU sends the selected head number on BUS00 and BUS01 from BC1 to BC8. The head number is validated by the FTH pulse (Y4 Figure 2-10) from BC3 to BC6 time. At FC8 time the Read signal is sent on BUS01.

2.22 SECTOR LOGIC

Each disc has slots that mark the beginning and end of the sectors, plus a slot that marks the beginning of the cylinder. These slots are detected by transducers that produce sector pulses (SEC) and index pulses (IND) and the logic is found on Figure 2-11. The four binary counters H5, G5, H6 and G6 count these pulses from each disc and the outputs from the counters drive two dual 4 input multiplexers G4 and H4. Outputs from the multiplexers are used to drive one

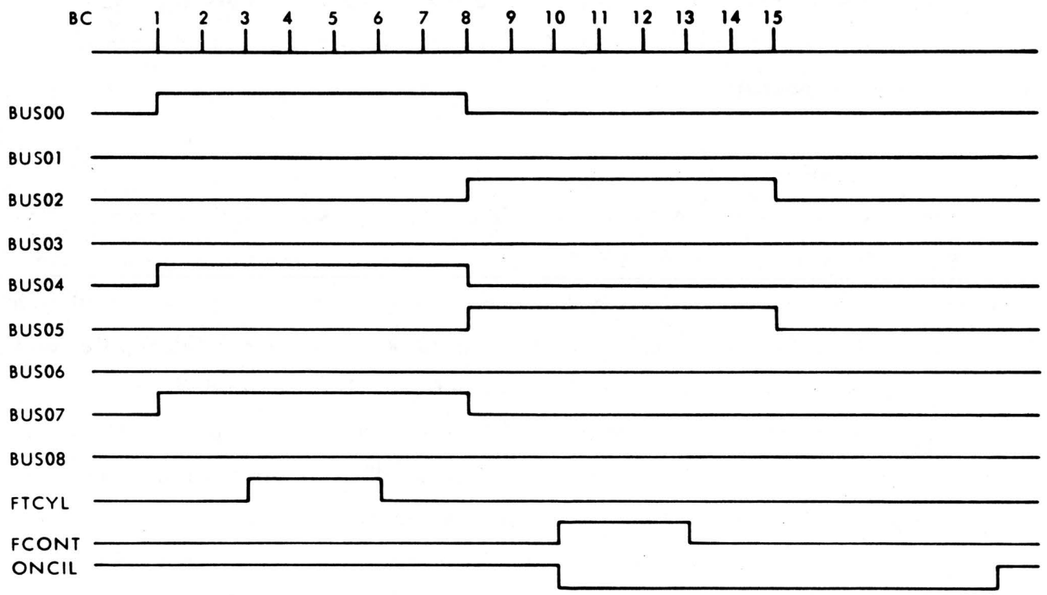


Figure 2-2 Seek Command Timing (Example Cylinder 145)

input to comparator H3 (the other input to the comparator comes from the sector address of the instruction via BUI02 to BUI05). When the two inputs are equal the output is used to set the FCOMP flip-flop S5. The clock for this flip-flop is the output from multiplexer H7.

2.23 WRITE DATA LOGIC

The main components of the write data logic are the data input buffer, the write data input selector, the write serializer, the write clock, the bit and format counters, and the write check word register.

2.24 Write Clock

Figure 2-3 shows the circuit of the write clock which is a crystal controlled 10 MHz oscillator. The output from the oscillator drives a JK flip-flop J5 whose output is a train of 100 ns pulses with a period of 200 ns. Output pin 6 sends clock pulses on the selected Write Data Line (WDL) unless they are inhibited by Nand gate N4 pin 6 or pin 8. The output from J5 pin 5 drives the other half of J5 whose outputs are 100 ns pulses with a period of 400 ns. Clock pulses WCP and WCP1 are produced from the output pin 9 and are used to control the write logic in the CU. The output from pin 7 is used to inhibit the clock pulse on WDL when a data 0 bit appears on WS15, and as the clock for flip-flop M5. This flip-flop inhibits WDL (when FBWG is active), so that the first write pulse and the clock pulse can be synchronized.

2.25 Bit Counter

This counter counts the 16 bits of each word and is formed by two 8-bit serial to parallel convertors V5 and W5 (Figure 2-11). Input to the counter is from flip-flop U8 and it is clocked by the trailing edge of either WCP or RCPA. The BC outputs from the counter are used to time the BUS logic and every 6.4 μs BC15 increments the format counter.

2.26 Format Counter

This counter is formed by two binary counters M8 and L8 (Figure 2-8) that are clocked by FCCN which is produced by BC15 and WCP1. The output from M8

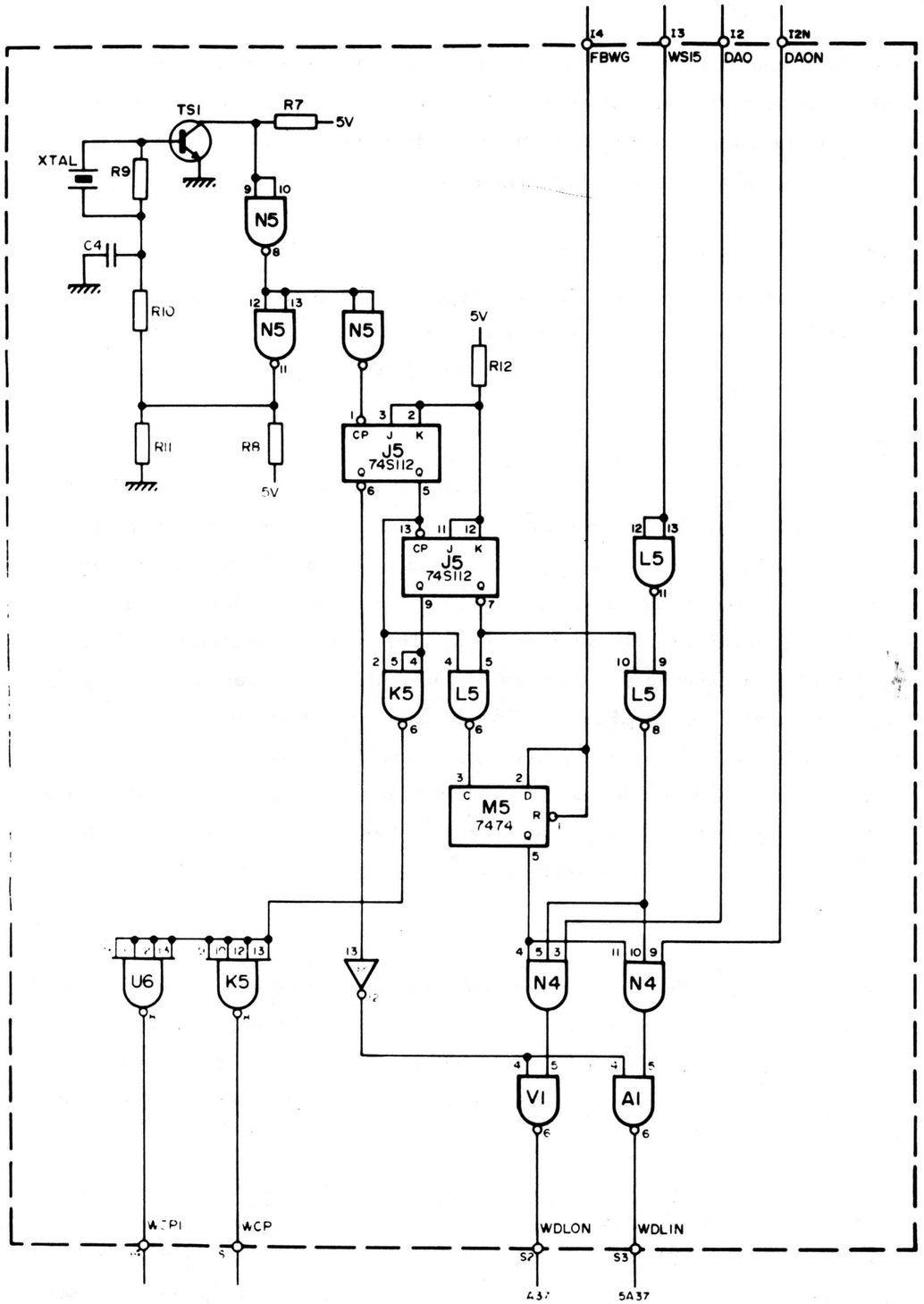


Figure 2-3 Write Clock Circuit

drives two 1-of-ten decoders N8 and N7 and the output from these together with the output from L8 produces the FC timing pulses that control the format of the read/write operations.

2.27 Data Input Buffer

The buffer uses four 4-word 4-bit register files M2, L2, K2 and J2 (Figure 2-9) to hold data from the BIO00 to BIO15 lines. Only two of the buffer's four word capacity are used and the address of the two buffers is provided by the output from flip-flop FIOR E6 (Figure 2-12). Each time an OTR is received FIOR toggles and with G3 active data is loaded into alternate buffers. Data is read out of the buffer that is addressed by the output from flip-flop FBC0 E6 (Figure 2-12) which is toggled each BC0 time. The buffer addressed by FBC0 is always the inverse of the buffer addressed by FIOR, so it is possible to load data into one buffer whilst reading from the other buffer. The outputs from the buffer are wired such that the bit positions of the data word are reversed.

2.28 Write Data Input Selector

The selector uses four quad 2-input multiplexers J4, K3, L4 and M3 (Figure 2-9) to enable either data from the buffer, the Write Check Word (WCW), or zeros to appear at the outputs. Inputs to the selector are enabled when Q7 pin 6 is low (0V) and the required input is selected by FC29N. When FC29N is high (5V) the data from the buffer is selected, and when FC29N is low (0V) the WCW data is selected. With Q7 pin 6 high (5V) data input is inhibited and the output from the selector will be all zeros.

2.29 Write Serializer

The serializer comprises two 8-bit parallel to serial convertors K4, and M4 (Figure 2-9). The serializer is loaded by WCPBC0N and the bit shift is enabled by WCP. The Preamble word is loaded at FC26 time when the output from the input selector has been inhibited and the ONE bit is provided via R4 pin 8. Output from the serializer is combined with the write clock pulses to record data on the selected disc, cylinder and sector.

2.30 Write Check Word Register

This register comprises two 8-bit serial to parallel convertors J3, L3 and the Exclusive OR gate E8 (Figure 2-9). The register is reset at FC26N time of a Write command and thereafter an Exclusive OR of all the data bits is made and stored in the register. After the last data word has been written, the contents of the register WCW are written on the disc at FC29N time.

2.31 Write Operation

When the CIO instruction has been received and accepted, the Write command is stored in the FWRITE flip-flop F2 (Figure 2-7), the sector address is stored in the data input buffer (Figure 2-9), the drive unit number is stored in the DA0 flip-flop (Figure 2-12), the BC and FC counters are reset and the CU switches into the EXT state. After the addressed sector has been found and FCOMP set (Figure 2-11), then:

- During FC0 time (BC0 to BC15 time), the selected head number is sent on BUS00 and BUS01 from BC1 to BC8 time and from BC3 to BC6 time this is validated by FTH.
- At FC1 time the write shift register is reset by FENN so that the multiplexer is filled with zeros for writing the synchronization area.
- From FC0 to FC8 time the GAP occurs because the write and erase flip-flops have not yet been set.
- At FC8 time the write enable flip-flop FBWG K7 and L7 (Figure 2-12) is set and enables the Write command to be sent on BUS00, the erase enable flip-flop FBRW R4 (Figure 2-12) is set and enables the Erase command to be sent on BUS04, and the control select flip-flop FCONT X5 and X6 (Figure 2-10) is set validating the Write and Erase commands.
- From FC8 to FC26 time zeros are serialized and written on the disc to form the synchronization area.
- At FC25 time the break request flip-flop FBR A2 (Figure 2-12) is set and the request is sent to the CPU asking for the first data word to be sent to the CU.
- At FC26 time the Preamble word is loaded into the write serializer and written on the disc.
- At FC27 time the first data word is serialized and written on the disc and further increments to the FC counter are inhibited by FC27 until the EOR signal on MAD03 is received. During this state the CU sends break request signals to the CPU and serializes and writes the data words of the record. When the EOR signal is received the EOR and FEOR flip-flops B6, validated by EORVALN F8 (Figure 2-12), are set which sets the FHALT flip-flop S5 that enables further increments to the FC counter.
- At FC28 time the last data word is serialized and written on the disc.
- At FC29 time the WCW is serialized and written on the disc.
- At FC30 time the Postamble word containing all zeros is written on the disc.
- At FC31 time the write enable flip-flop FBWG is reset, but the erase enable FBRW remains set to create the erase delay to the end of the record, during which time the FC counter is incremented up to FC37 time.
- At FC37 time the erase and control select flip-flop FBRW and FCONT are reset and the CU switches into the WST state.

Figure 2-4 shows the timing for a write operation.

2.32 READ DATA LOGIC

The main components of the read data logic are the read clock, the read deserializer, the data buffer, the output selector, and the read check word register.

2.33 Read Clock

Figure 2-5 shows the circuit of the read clock whose input is the clock and data pulses (RDL) from the selected disc. L6 is a single shot multivibrator that suppresses the data pulses and produces the RCPA and RCPB clock pulses that control the read logic; these clock pulses are 100 ns (adjusted by P1) with a period of 400 ns. Q6 is a single shot multivibrator that suppresses the clock pulses (from RDL) and produces the data ONE pulses (RD). When flip-flop FRENA U8 (Figure 2-12) is active, both the clock and data pulses are enabled to the CU read data logic.

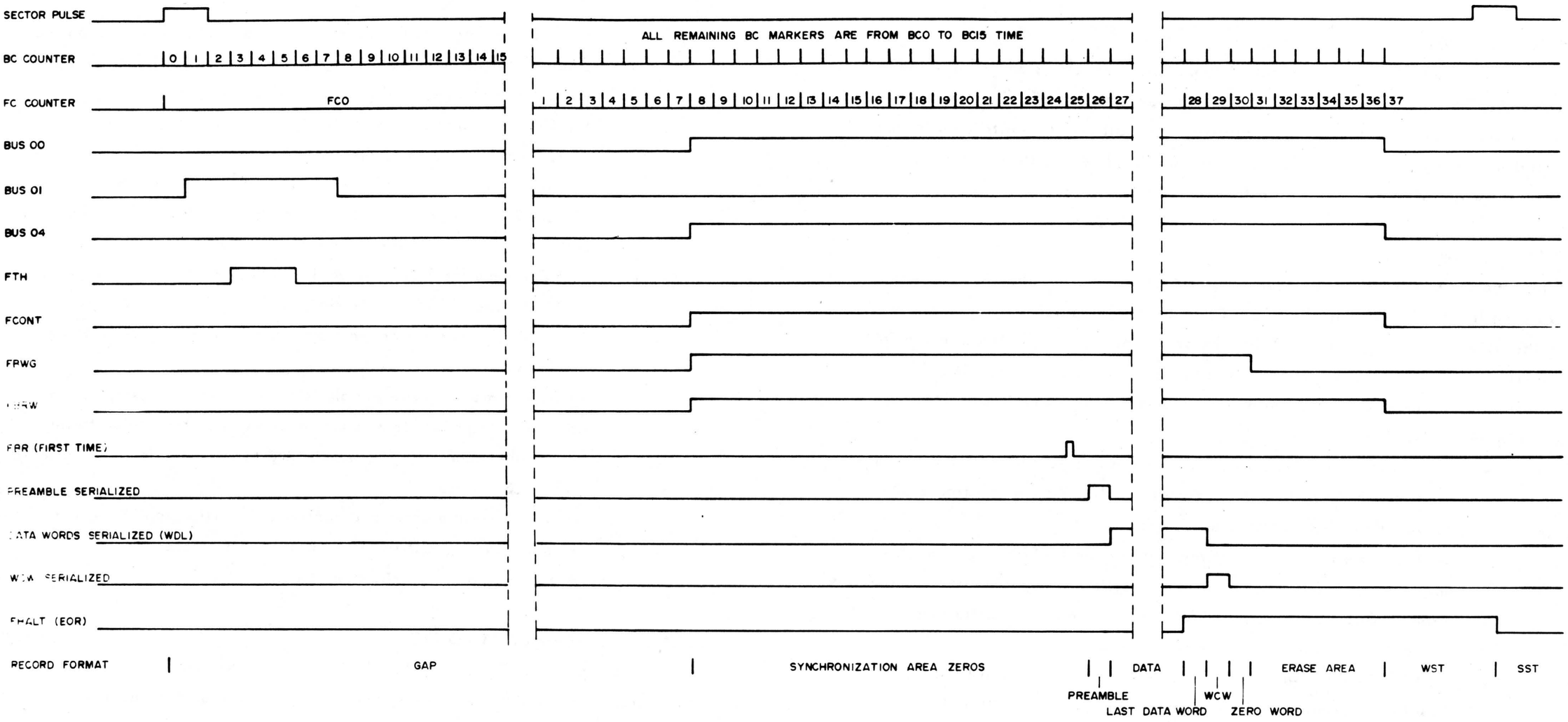


Figure 2-4 Write Operation Timing (Write Head No 2)

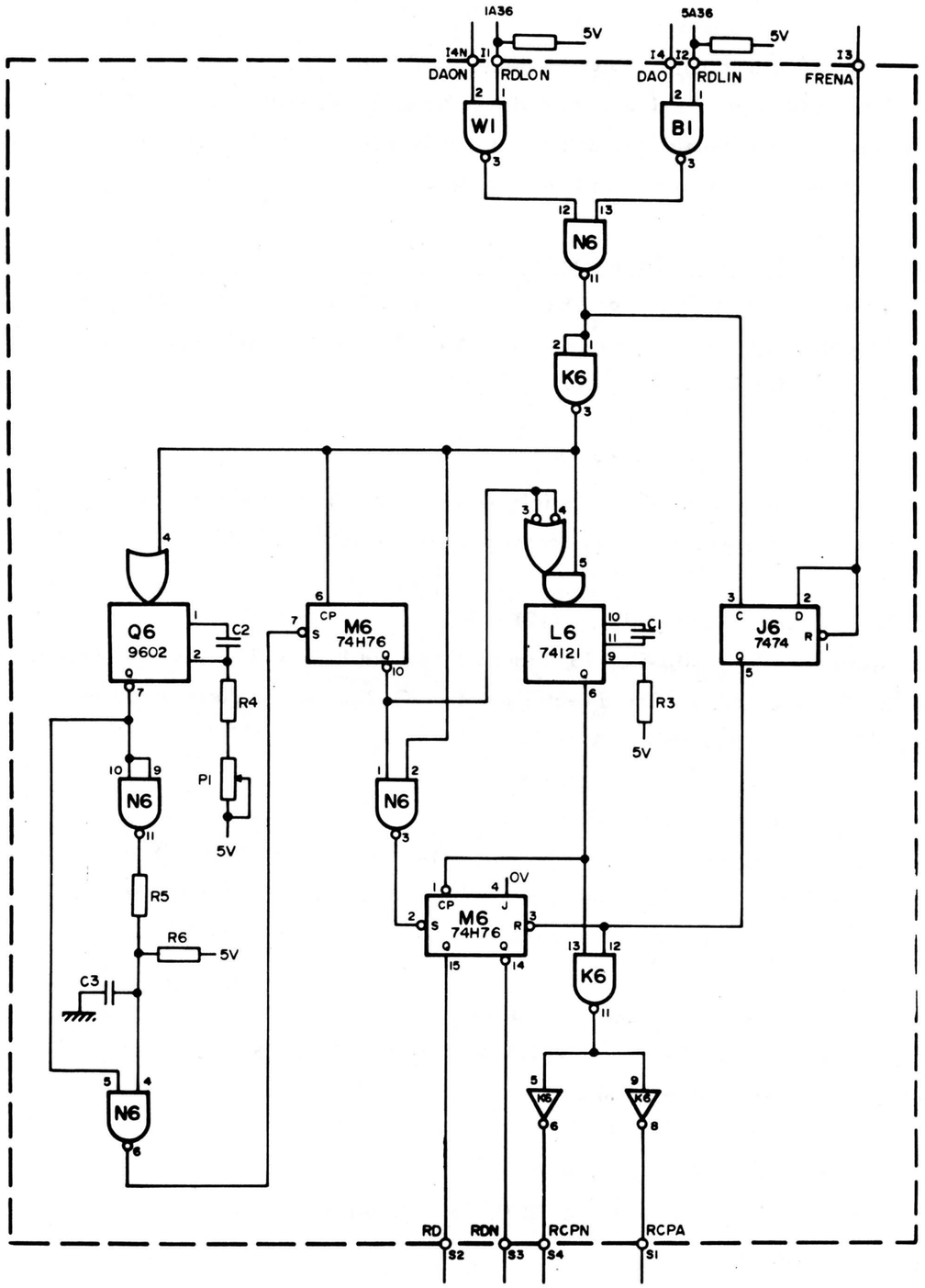


Figure 2-5 Read Clock Circuit

2.34 Read Deserializer

The deserializer comprises two 8-bit serial to parallel convertors P4 and Q4 (Figure 2-13). Data is loaded into the deserializer by RCPB and at BCOA time it is clocked into the data buffer.

2.35 Data Buffer

The buffer uses four 4-word 4-bit register files N3, P3, Q3 and R3 (Figure 2-13) to hold data from the Read deserializer. Only two of the buffer's four word capacity are used and the address of these two buffers is provided by the FBCON output from flip-flop E6 (Figure 2-12). Each BC0 time the flip-flop toggles and, with U4 active, data is loaded into alternate buffers. Data is read out of the buffer that is addressed by the output from flip-flop FIOR E6 (Figure 2-12) which is toggled each time an INR is received. The buffer addressed by FIOR is always the inverse of the buffer addressed by FBCON, so it is possible to load data into one buffer whilst reading from the other buffer. Output from the buffer is loaded into the Output Selector.

2.36 Output Selector

The selector uses four quad 2-input multiplexers N2, P2, Q2 and R2 (Figure 2-13) to enable either data from the buffer or the outputs from the status flip-flops to be sent to the CPU. Inputs from the data buffer are enabled if the CU is not in the WST state. When the CPU switches into the WST state the outputs from the status flip-flops are enabled. Gating onto the BIO lines is enabled by TMP.

2.37 Read Check Word (RCW) Register

The register comprises two 8-bit serial to parallel convertors X8, Y8, and the Exclusive OR gate V4 (Figure 2-14). The register is reset when the preamble detection flip-flop FPRE V8 is set by the preamble bit. An Exclusive OR of all the data bits (including the WCW) is made and if the result for the record is not zero, the data fault flip-flop FST13 is set.

2.38 Read Operation

When the CIO instruction has been received and accepted, the Read command is stored in the FWRITE flip-flop F2 (Figure 2-7), the sector address is stored in the data input buffer (Figure 2-9), the drive unit number is stored in the DA0 flip-flop

(Figure 2-12), the BC and FC counters are reset, and the CU switches into the EXT state. After the addressed sector has been found and FCOMP set (Figure 2-11) then:

- During FC0 (BC0 to BC15 time), the selected head number is sent on BUS00 and BUS01 from BC1 to BC8 time and from BC3 to BC6 time this is validated by FTH.
- At FC8 time the read enable flip-flop FBRW K7 and L7 (Figure 2-12) is set and enables the Read command to be sent on BUS01, and the control select flip-flop FCONT X5 and X6 (Figure 2-10) is set validating the Read command.
- At FC19 time (in the theoretical middle of the synchronization area) the read data line flip-flop FRENA U8 (Figure 2-12) is set and the read clock starts to sample the data line RDL. The BC and FC counters are reset and the CU waits until the reamble is detected.
- The Preamble ONE bit sets the Preamble detection flip-flop FPRE V8 (Figure 2-14) that resets the RCW register and restarts the BC counter.
- The BC counter counts the RCP pulses and each BC0 time a word has been read, deserialized, loaded into the data buffer, and the break request flip-flop FBR set to ask for a data exchange with the CPU until the EOR signal on MAD03 sets the FHALT flip-flop B6 (Figure 2-12).
- If the RCW total is zero the CU switches into the WST state without setting the data fault flip-flop FST13.

Figure 2-6 shows the timing for a read operation.

2.39 STATUS WORD LOGIC

The status word bits are provided by status flip-flops and logic levels and they indicate the operability, error, and other conditions or states of the CU. One or more bits will be sent to the CPU, via the BIO lines, in response to either a TST or SST instruction. The status bits are enabled through the output selector (Figure 2-13) by WST and are gated onto the BIO lines by TMP.

2.40 Not Operable (FST15)

The status is held in flip-flop G8 (Figure 2-14) and it is set via the four bit latch J8 and the quad 2-input multiplexer K8 (Figure 2-10) when an UNSAFE signal is received from either drive unit. It is reset by CLERN after the fault condition on the drive unit has been cleared.

2.41 Throughput Error (FST14)

The status is held in flip-flop W3 (Figure 2-14) and it is set if the FBR flip-flop A2 (Figure 2-12) has not been reset within 12.8 μ s of the exchange request being sent to the CPU. It is reset by SCANAN.

2.42 Data Fault (FST13)

The status is held in flip-flop W3 (Figure 2-14) and it is set if the RCW total is not zero at the end of a read operation. It is reset by SCANAN.

2.43 Incorrect Length (FST12)

The status is held in flip-flop T3 (Figure 2-14) and it is set if either FRENAN or FBWGN are active when a sector pulse (SEC) is detected during read/write operations. It is reset by SCANAN.

2.44 Program Error (FST11)

The status is held in flip-flop T3 (Figure 2-14) and it is set if an INR instruction is received, from the IOP, during a write operation or an OTR instruction is received, from the IOP, during a read operation. It is reset by SCANAN.

2.45 Drive Unit Number (BIO09)

The status is held in C5 (Figure 2-12) the DA0 flip-flop that is used to activate the selected drive unit.

2.46 Disc Selected (BIO08)

The status is held in F2 (Figure 2-7) the DA1 flip-flop that is used to activate the select disc logic.

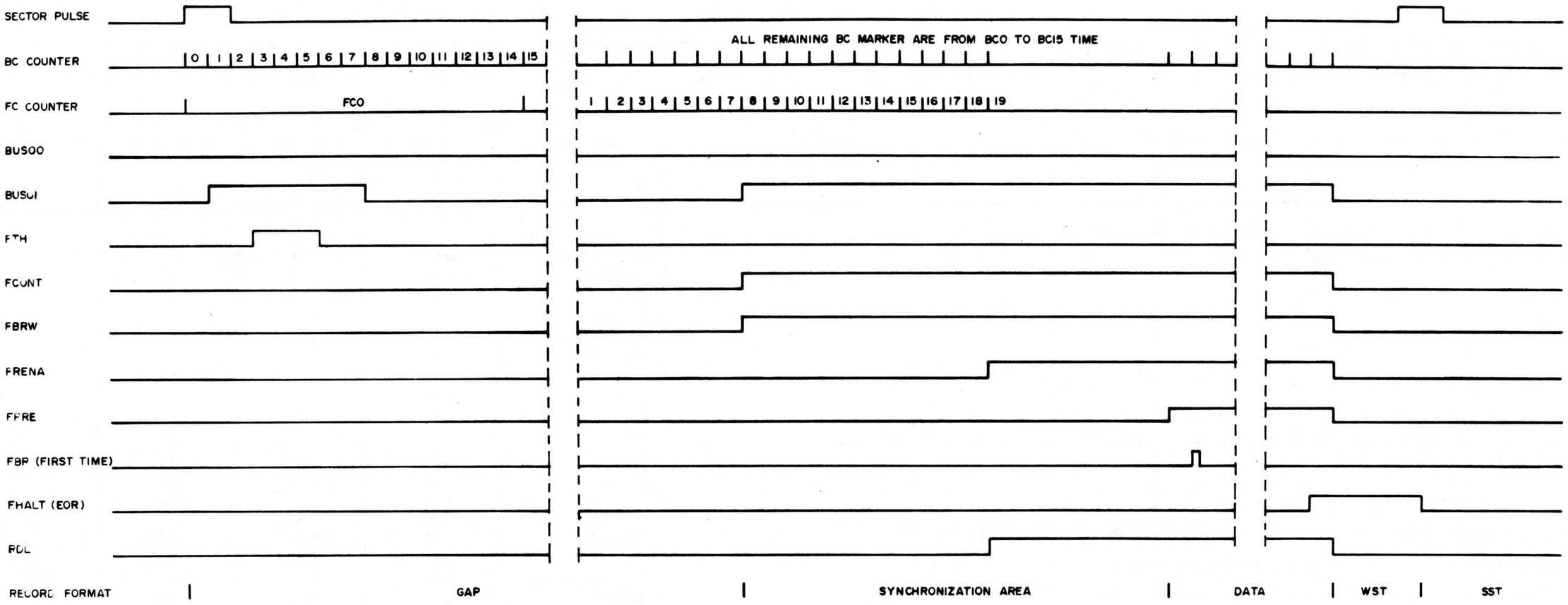


Figure 2-6 Read Operation Timing (Read Head No 2)

2.47 Seek Error (FST06)

The status is held in flip-flop U3 (Figure 2-14) and it is set if the Seek command has finished (SK) but has not been executed correctly (RER from the drive unit) or the drive unit becomes inoperable (FNOP). The logic for these three error conditions is on Figure 2-10. Reset is by CLRN.

2.48 Seek Complete (FST05)

The status is held in flip-flop V3 (Figure 2-14) and it is set, when the Seek command has finished and the head is ON cylinder, by SK and ONCIL K8 (Figure 2-10). Reset is by CLRN.

2.49 Was Unready (FST01)

The status is held in flip-flop V3 (Figure 2-14) and it is set when a drive unit that was unready, e.g. after power ON, discpack exchanged and START button pushed, sends the RDY signal (Figure 2-10) during scanning. It is reset by CLRN.

2.50 INTERRUPT/BREAK REQUEST LOGIC

The break request logic is shown in Figure 2-12 (A2) and the flip-flop is set during read/write operations to request a data exchange for each data word of the record. These requests are answered with either an INR (read) or OTR (write) instruction from the IOP. The BRLN line is connected direct to the IOP and its priority level is hardwired on the back of connector 4 (on the IOP card) at system installation time.

The interrupt logic is shown in Figure 2-8 and the flip-flop U3 is set each time the CU goes into the WST state e.g. end of read/write operation, end of Seek command etc. The output from this flip-flop enables the priority code of the BIEC lines (set by the selector switches E1 at system installation time) to be sent to the CPU. When the priority level is higher than any other interrupt (i.e. 0 is the highest, 63 is the lowest) the CPU responds by sending an SST instruction to the CU. The CU responds to the SST by sending the status word bits to the CPU.

2.51 DRIVE UNIT INTERFACE CONNECTIONS

The corresponding pin connections between the CU and the drive units are made with twisted pairs and are shown in Table 2-2.

Table 2-2 Interface Connections

Signal Name	CU Connector To Drive Unit 0	CU Connector To Drive Unit 1	Drive Unit Connector
BUS00N	1A25	5A25	48
Signal Ground	1B25	5B25	51
BUS01N	1A26	5A26	47
Signal Ground	1B26	5B26	50
BUS02N	1A27	5A27	46
Signal Ground	1B27	5B27	49
BUS03N	1A13	5A13	54
Signal Ground	1B13	5B13	57
BUS04N	1A12	5A12	53
Signal Ground	1B12	5B12	56
BUS05N	1A11	5A11	52
Signal Ground	1B11	5B11	55
BUS06N	1A35	5A35	60
Signal Ground	1B35	5B35	64
BUS07N	1A34	5A34	59
Signal Ground	1B34	5B34	63
BUS08N	1A10	5A10	40
Signal Ground	1B10	5B10	43
SEL N	1A07	5A07	36
Signal Ground	1B07	5B07	39
FTCYL N	1A04	5A04	10
Signal Ground	1B04	5B04	13
FTH N	1A05	5A05	11
Signal Ground	1B05	5B05	14
FCONT N	1A33	5A33	17
Signal Ground	1B33	5B33	21
WDL N	1A37	5A37	8
Signal Ground	1B37	5B37	12
UNSAFE N	1A02	5A02	34
Signal Ground	1B02	5B02	37
RER N	1A03	5A03	3
Signal Ground	1B03	5B03	7
SEC 0N	1A06	5A06	23
Signal Ground	1B06	5B06	26
SEC 1N	1A29	5A29	30
Signal Ground	1B29	5B29	33

Signal Name	CU Connector To Drive Unit 0	CU Connector To Drive Unit 1	Drive Unit Connector
IND 0N	1A08	5A08	24
Signal Ground	1B08	5B08	27
IND 1N	1A30	5A30	35
Signal Ground	1B30	5B30	38
RDY N	1A31	5A31	2
Signal Ground	1B31	5B31	5
ONCIL N	1A32	5A32	29
Signal Ground	1B32	5B32	32
RDL N	1A36	5A36	1
Signal Ground	1B36	5B36	4
Mechanical Gnd.	1A01	5A01	59

2.52 RESET LOGIC

If a power failure occurs in the CPU during a disc operation it is necessary to de-select the logic in the drive unit. This is done via the RSLN signal from the CPU and gates T1 and B2 (Figure 2-8); the same signal and logic sends the select signal to the drive unit after the power is restored.

2.53 LOGIC DIAGRAMS AND CARD COMPONENTS

The logic diagrams for the CU are Figures 2-7 to 2-14 and were derived from Boolean Book 5111 991 06562 dated 750228.

Figure 2-15 shows the component layout of the control unit and Table 2-3 lists the components.

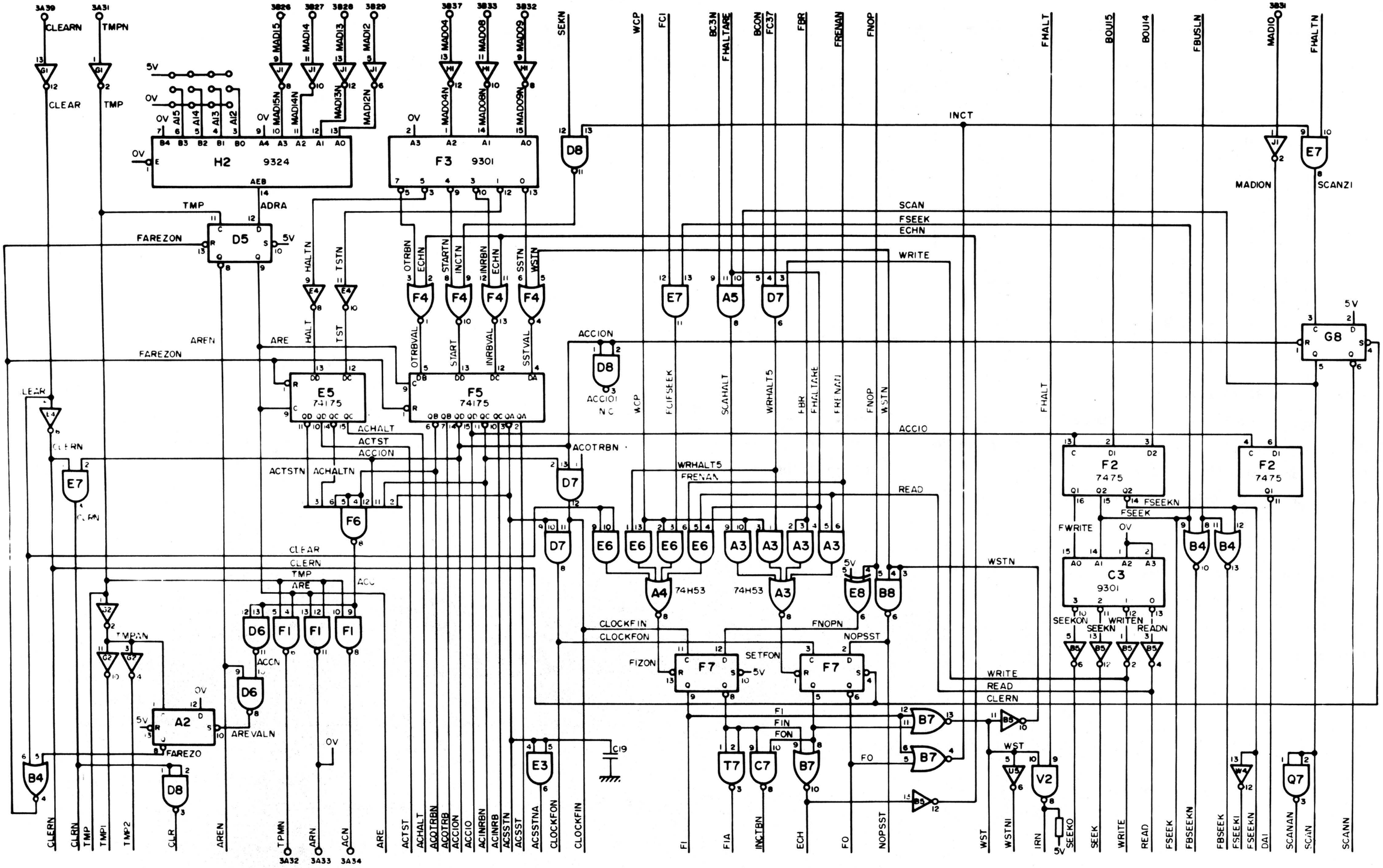


Figure 2-7 Logic Diagram

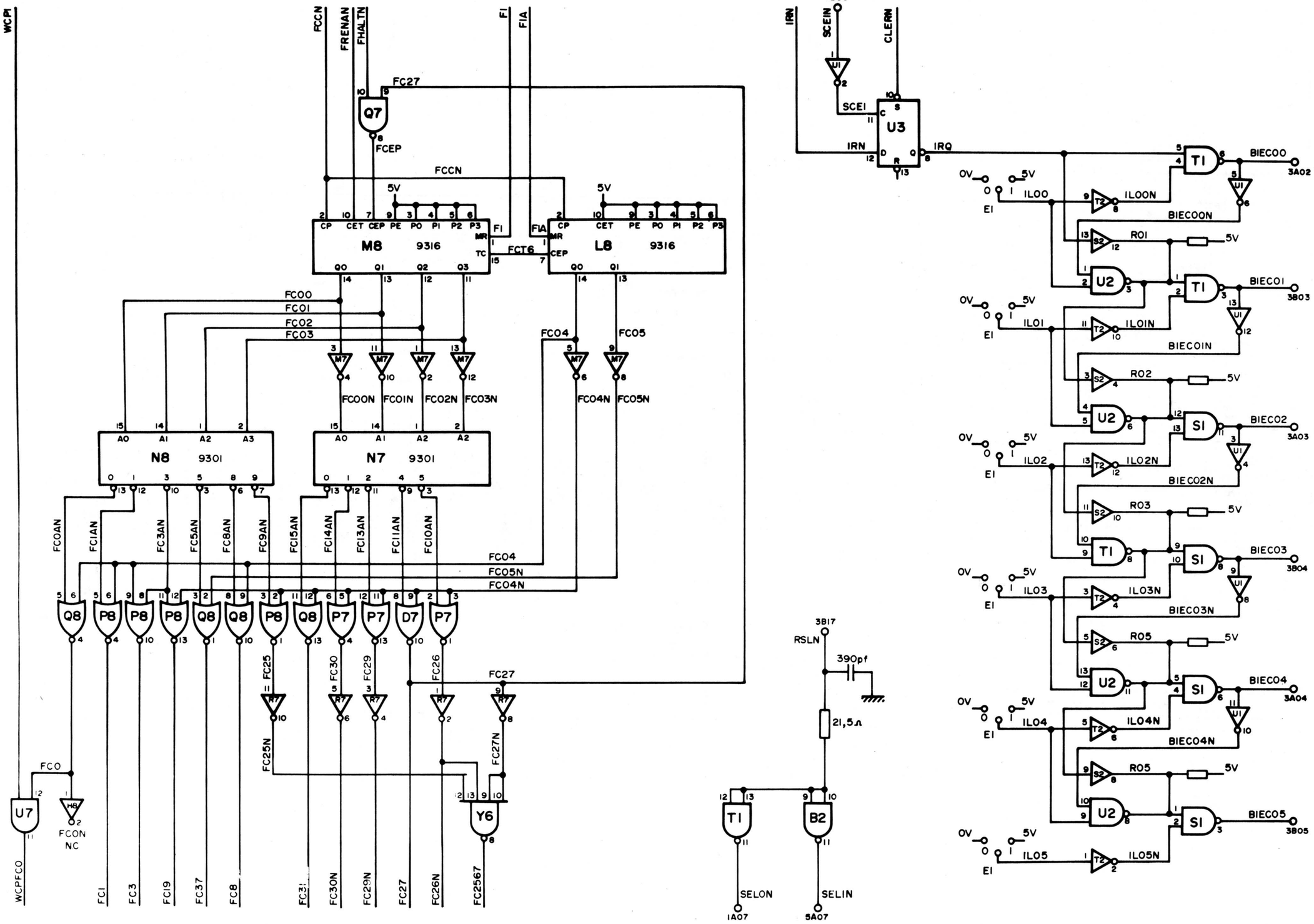


Figure 2-8 Logic Diagram

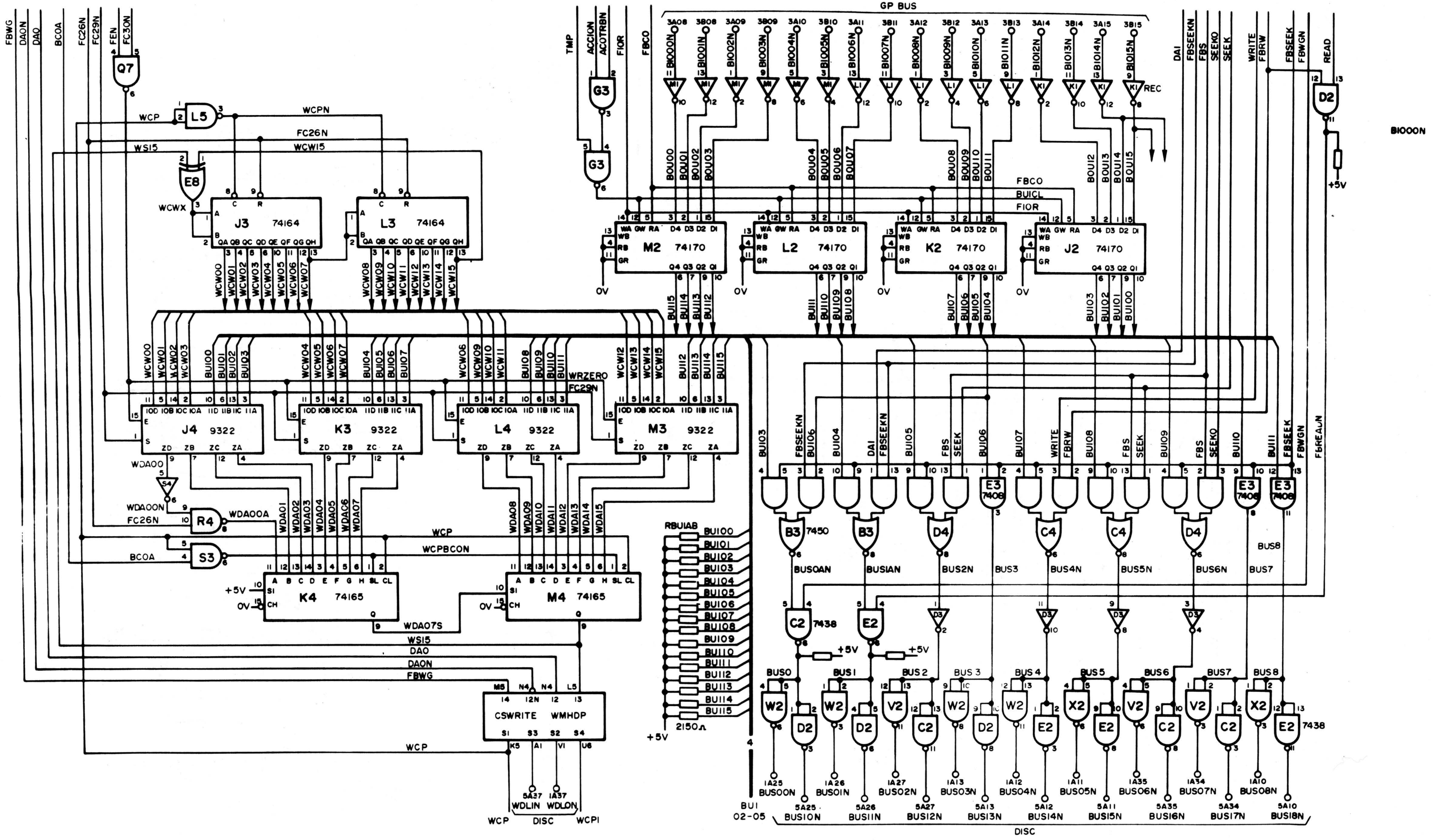
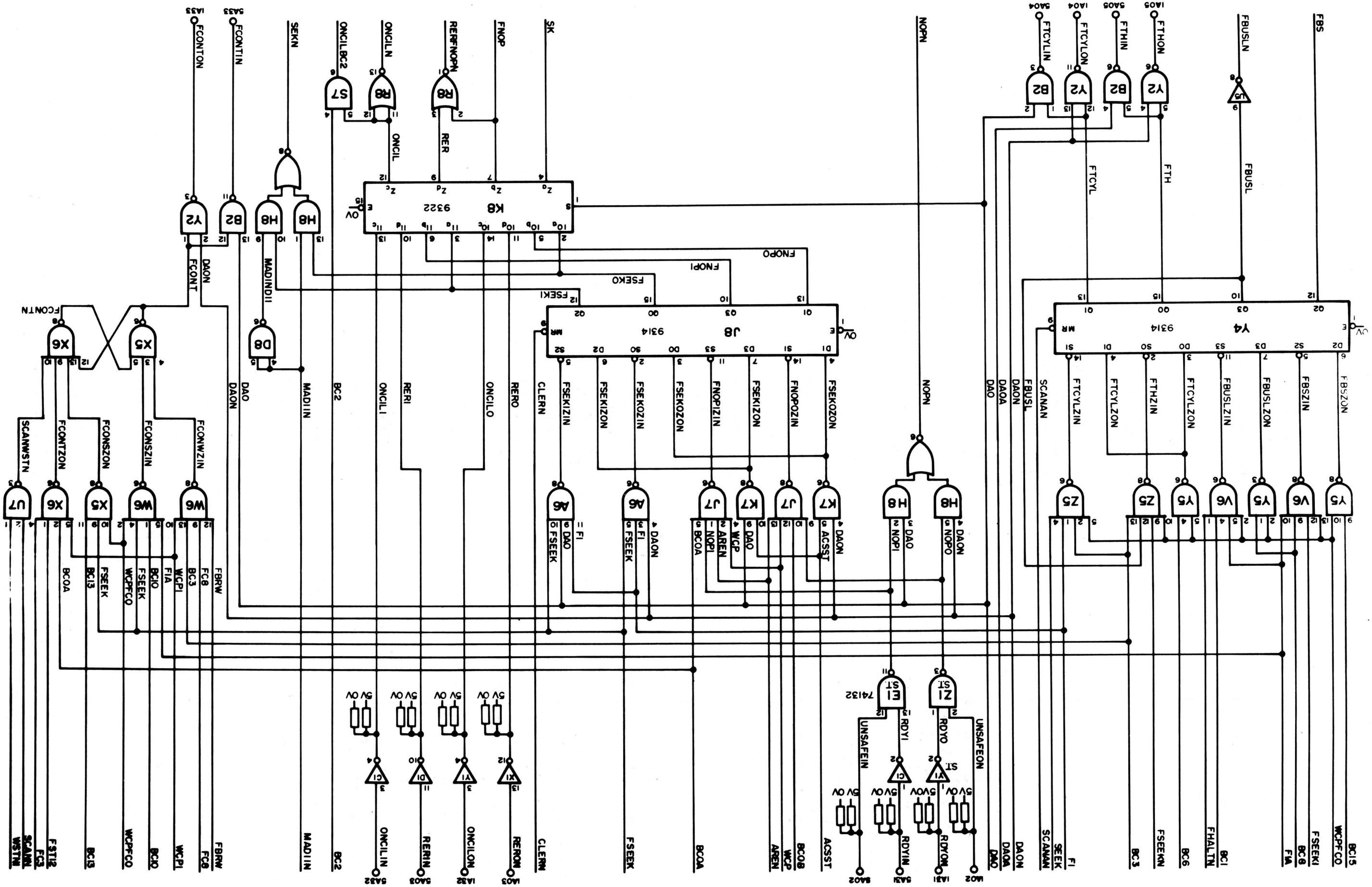


Figure 2-9 Logic Diagram

Figure 2-10 Logic Diagram



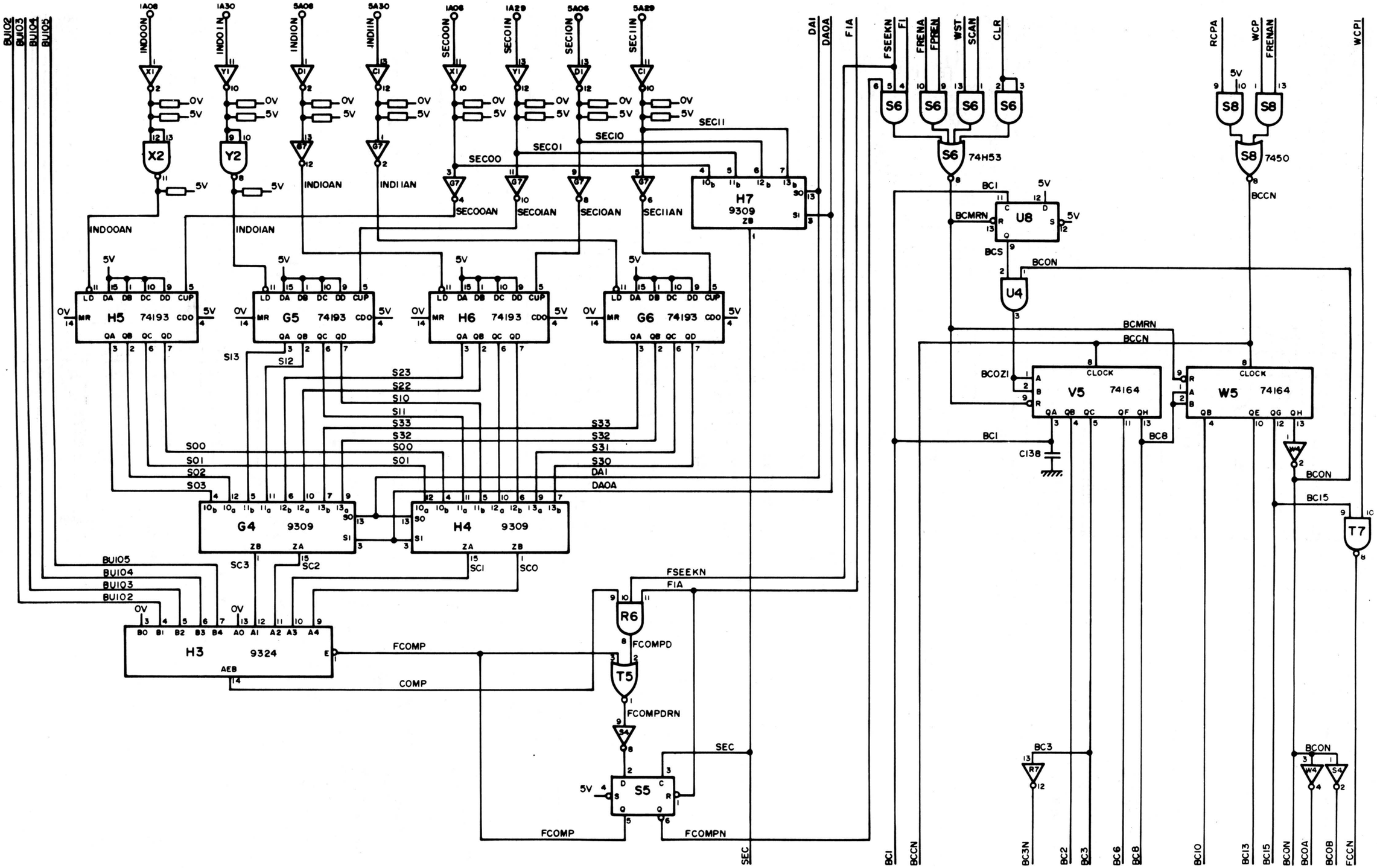


Figure 2-11 Logic Diagram

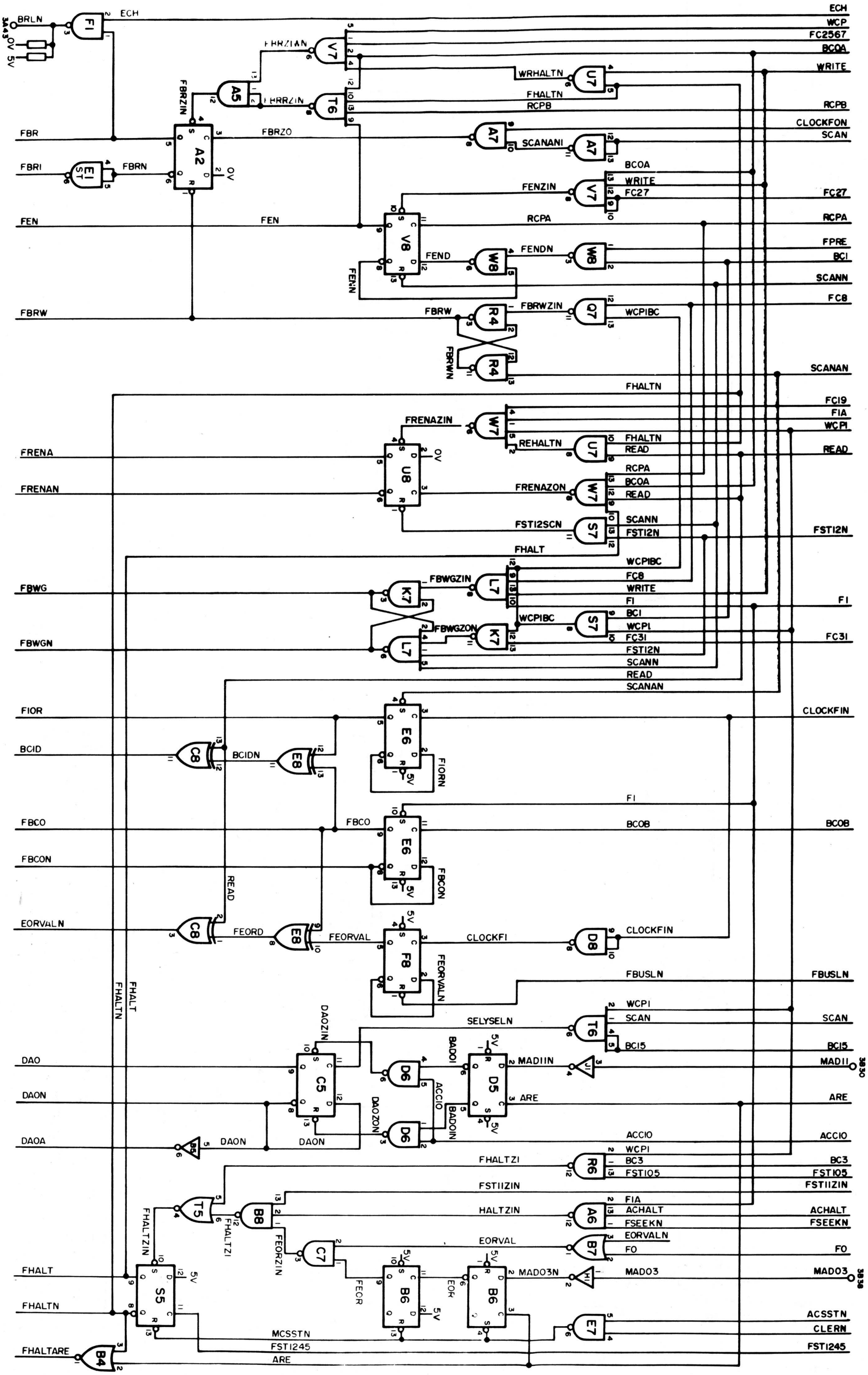


Figure 2-12 Logic Diagram

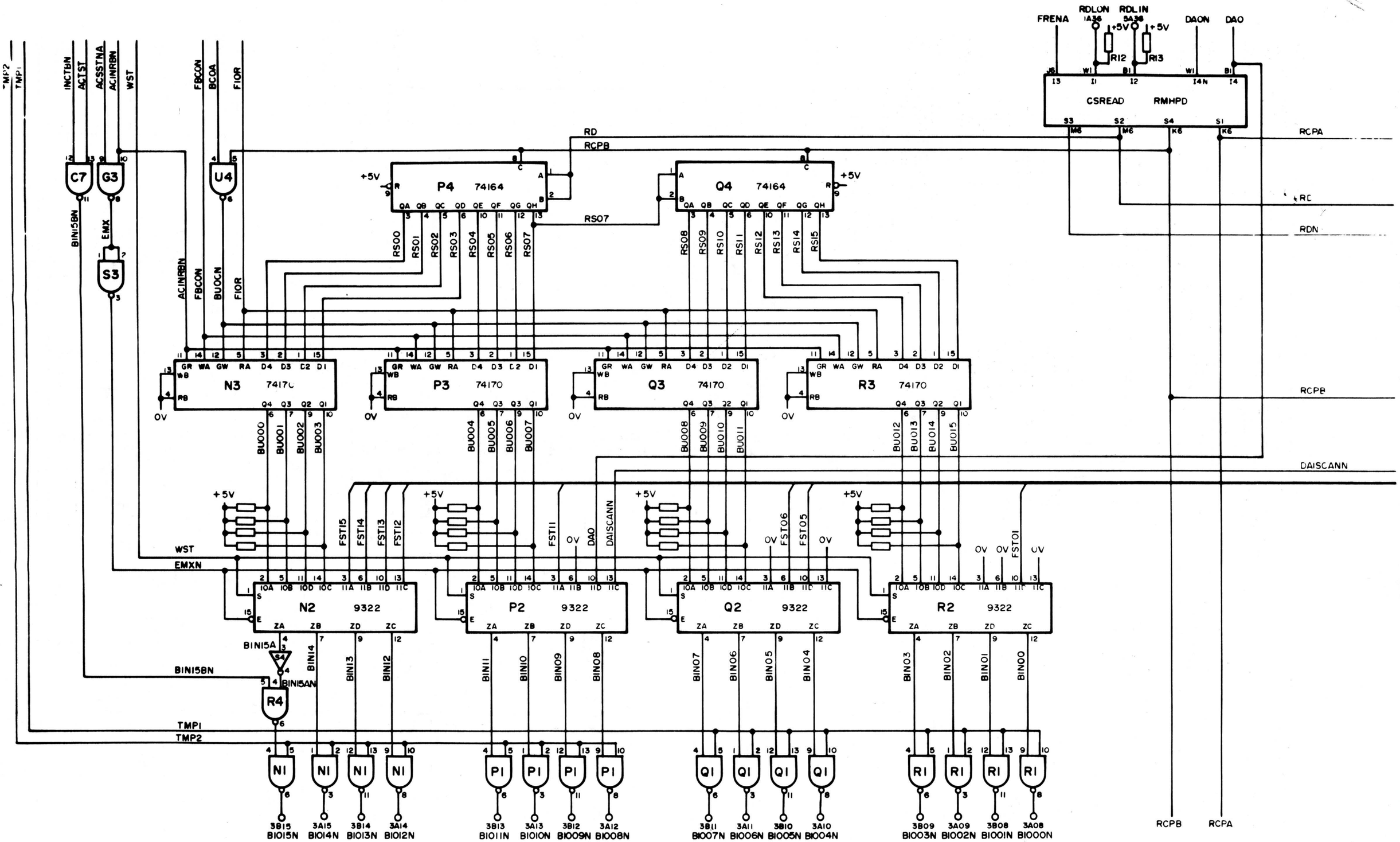


Figure 2-13 Logic Diagram

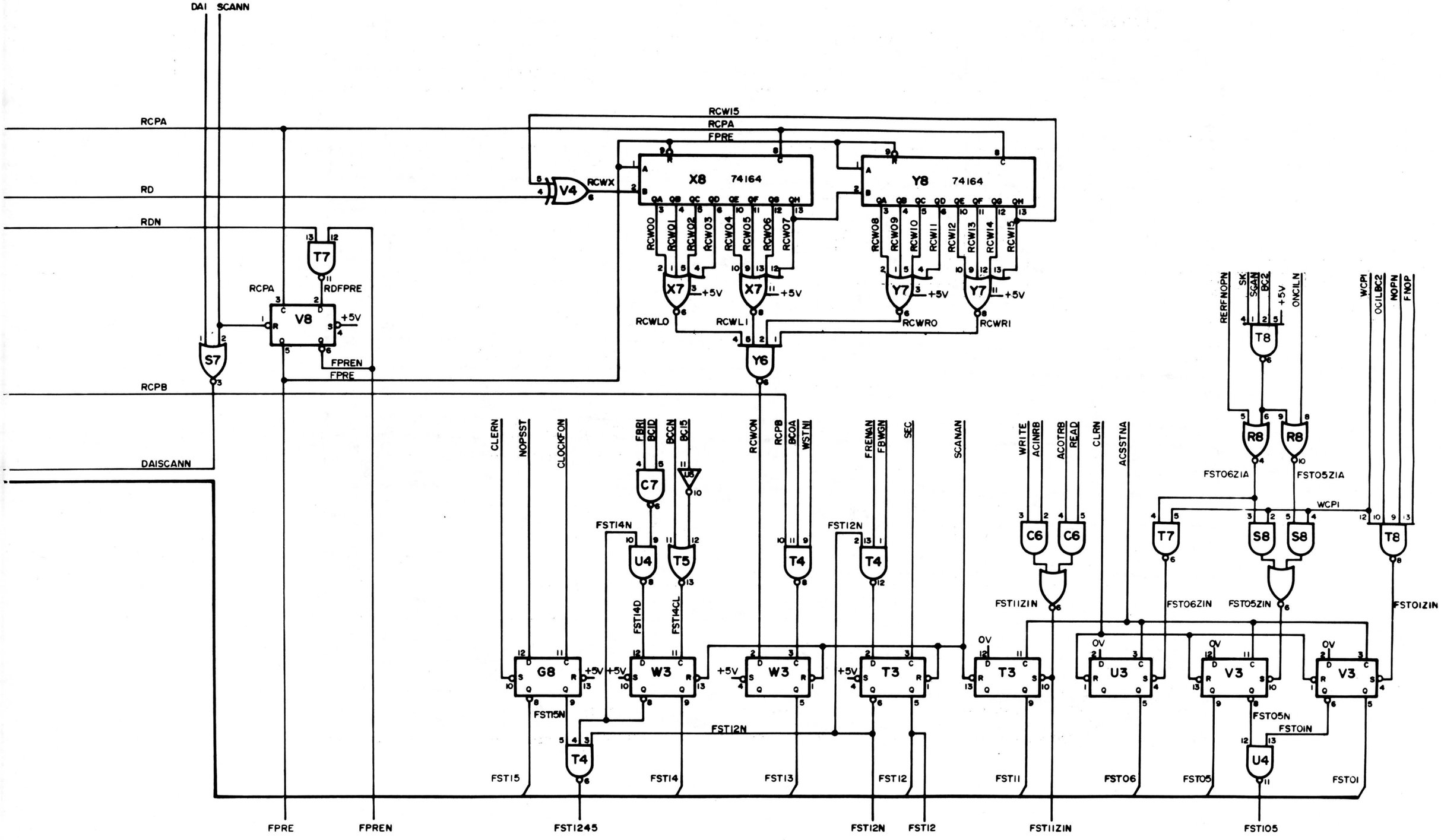


Figure 2-14 Logic Diagram

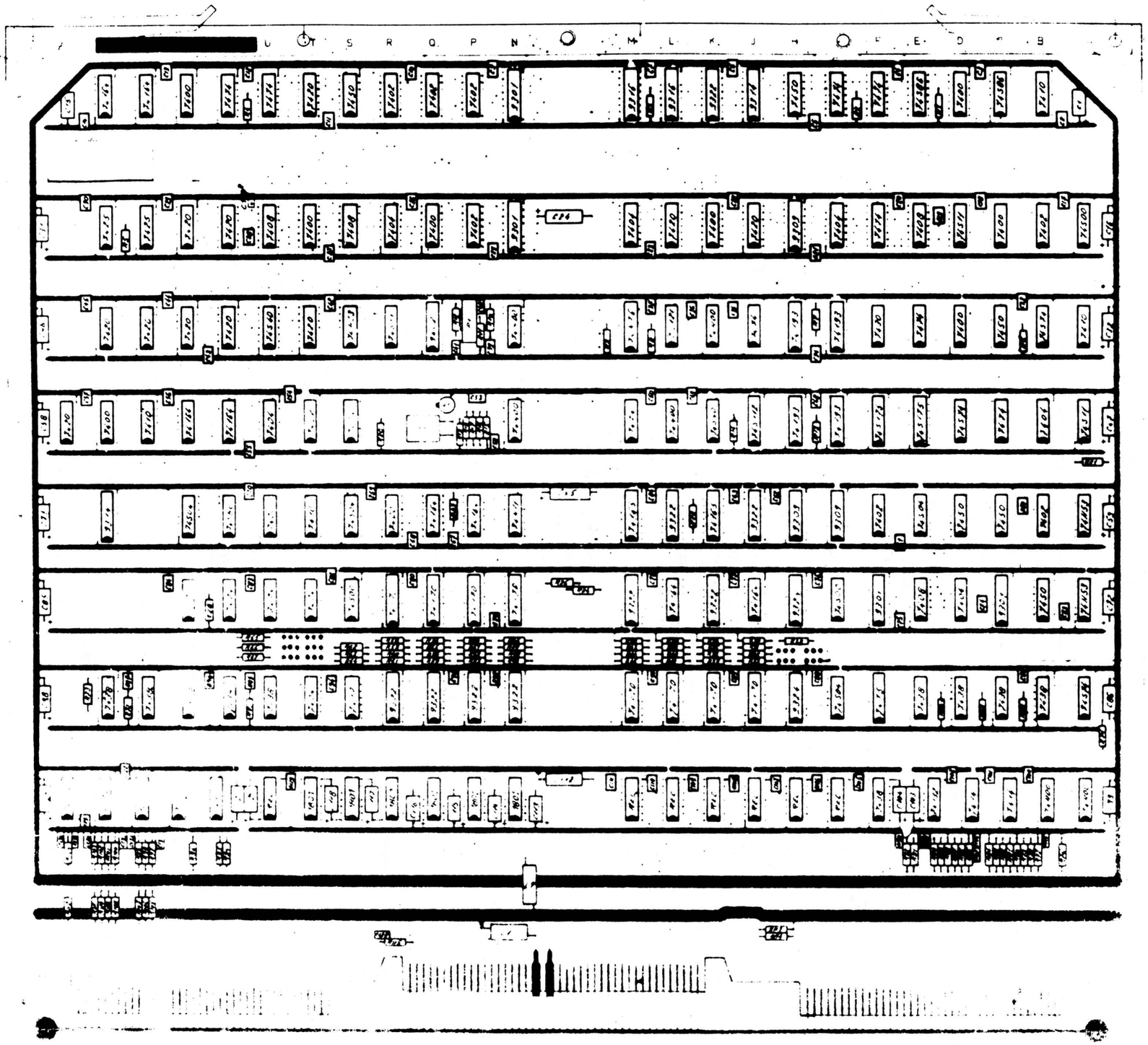


Figure 2-15 Component Layout of Control Unit

Table 2-3 List of Components

Reference	Description	12NC Code
Printed Circuit		5111 100 05603
C7,D6,D8,K7,Q7,R4,T7,U4,W8,Y5.	Integrated Circuit 7400	
A1,B1,K6,L5,N5,N6,V1,W1.	Integrated Circuit 74H00	
A7,G3,S3.	Integrated Circuit 74S00	
B4,B7,F4,P7,P8,Q8,R8,T5.	Integrated Circuit 7402	
B5,D3,G7,M7,R7,T2,U5.	Integrated Circuit 7404	
E4,G2,S4,W4.	Integrated Circuit 74S04	
E3,E7,S7,U7.	Integrated Circuit 7408	
T4,X5,A6,B8.	Integrated Circuit 7410	
N4.	Integrated Circuit 74H11	
A5,D7,R6.	Integrated Circuit 74S11	
C1,D1,X1,Y1.	Integrated Circuit 7414	
S2.	Integrated Circuit 7417	
J7,L7,T6,T8,V6,V7,W6,W7,X6,Y6,Z5.	Integrated Circuit 7420	
X7,Y7.	Integrated Circuit 7425	
F6.	Integrated Circuit 7430	
B2,C2,D2,E2,F1,U2,V2,W2,X2,Y2.	Integrated Circuit 7438	
K5,U6.	Integrated Circuit 74S40	
B3,C4,C6,D4,H8,S8.	Integrated Circuit 7450	
A3,A4,S6.	Integrated Circuit 74H53	
G5,E6,F7,F8,G8,J6,M5,S5,T3,U3,U8,V3, V8,W3.	Integrated Circuit 7474	
A2,B6,D5.	Integrated Circuit 74S74	
F2.	Integrated Circuit 7475	
M6.	Integrated Circuit 74H76	
C8,E8,V4.	Integrated Circuit 74S86	
J5.	Integrated Circuit 74S112	
L6.	Integrated Circuit 74121	
E1,Z1.	Integrated Circuit 74132	
J3,L3,P4,Q4,V5,W5,X8,Y8.	Integrated Circuit 74164	
K4, M4.	Integrated Circuit 74165	
J2,K2,L2,M2,N3,P3,Q3,R3.	Integrated Circuit 74170	
E5,F5.	Integrated Circuit 74S175	
G5,G6,H5,H6.	Integrated Circuit 74193	
G1,H1,J1,K1,L1,M1,U1.	Integrated Circuit REC 0612	
C3,F3,N7,N8.	Integrated Circuit 9301	
G4,H4,H7.	Integrated Circuit 9309	
J8,Y4.	Integrated Circuit 9314	
L8,M8.	Integrated Circuit 9316	
J4,K3,K8,L4,N2,P2,Q2,R2.	Integrated Circuit 9322	
H2,H3.	Integrated Circuit 9324	
Q6	Integrated Circuit 9602	
C112	Capacitor 33µF, 10V, CTS13.	
C1,15,16,31,32,46,47,58,59,71,72,85, 86,98,99,103,121.	Capacitor 10µF, 25V FITCO.	
C104,113-118,120.	Capacitor 3.3µF, 16V, CTS13.	
C2-7,9-14,17,18,20-23,33-36,39,42-45, 48-50,52,54-57,60-64,67-70,73-80,82-84,87-90,92-97,100-102,105-111,119, 122,123,125-136.	Capacitor 0.01µF, cer.plat.	
C40.	Capacitor 150pF, 63V, ±2%, cer.plat.	
C53.	Capacitor 1000pF, 100V, ±10%, cer.plat.	
C137.	Capacitor 3900pF, 100V, ±10%, cer.plat.	
C37,41.	Capacitor 21.5pF, 400V, ±1%, CA115.	
Q1.	Transistor BSX20	
Y1.	Quartz QA 60A 10 000 KHZ	
L1,L2.	Self	
R24,77,80,81,84,85,88,89,92,94,97-104.	Resistor 147Ω, 1/8W, ±1%.	
R25,78,79,82,83,86,87,90,91,95,105-112.	Resistor 562Ω, 1/8W, ±1%.	
R76,96.	Resistor 3.83KΩ, 1/8W, ±1%.	
R115.	Resistor 21.5Ω, 1/8W, ±1%.	
R18,19.	Resistor 3.16KΩ, 1/8W, ±1%.	
R17.	Resistor 1.12KΩ, 1/8W, ±1%.	
R11.	Resistor 5.11KΩ, 1/8W, ±1%.	
R10.	Resistor 261Ω, 1/8W, ±1%.	
R15.	Resistor 464Ω, 1/8W, ±1%.	
R16.	Resistor 681Ω, 1/8W, ±1%.	
R8.	Resistor 6.81KΩ, 1/8W, ±1%.	
R12,30-61.	Resistor 2.15KΩ, 1/8W, ±1%.	
R1-7,9,13,14,20-23,28,29,62-74.	Resistor 1KΩ, 1/4W, ±5%.	
P1.	Potentiometer 2600P 203 20K	
N1,P1,Q1,R1,S1,T1.	Integrated Circuit 1801	
R113.	Resistor 220Ω, 1/4W, 5%.	
R114.	Resistor 390Ω, 1/4W, 5%.	
C19,138.	Capacitor 470pF, 10%, cer.plat.	